◇STRUCTURE Silicon Monolithic Integrated Circuit
◇PRODUCT NAME 256 x 16 bit Electrically Erasable Programmable ROM
◇PART NUMBER BR93L66/F/RF/FJ/RFJ/FV/RFV/RFVM-W
◇OUTLINE DIMENSION Fig. - 1 (Plastic Mold)
◇BLOCK DIAGRAM Fig. - 2
◇FUNCTION General purpose
◇FEATURES
- 256words x 16 bit organization 4kbit serial EEPROM
- Wide operating supply voltage range(1.8～5.5V)
- Three wire serial interface
- Auto-increment of registers address for Read mode
- Prevent inadvertent writing
  - Defaults to power up with write-disabled state
  - Software instructions for write-enable/disable
  - Write inhibit at low Vcc
- Automatic erase-before write and self-timed programming cycle
- Read/$\overline{\text{Busy}}$ Status
- Low Power Consumption
  - Write (5V) : 1.2mA(Typ.)
  - Read (5V) : 0.3mA(Typ.)
  - Standby (5V) : 0.1 μ A(Typ.)
- Full TTL compatible input and output
- Space Saving DIP/SOP/SOP-J/SSOP-B/MSOP8pin Package
- High reliability fine pattern CMOS technology
- 40 Years Data Retention
- 1,000,000 Write/Erase Cycle
- Initial data FFFFh in all address

◇ABSOLUTE MAXIMUM RATINGS(Ta=25°C)

Parameter	Symbol	Rating		Unit
Supply Voltage	Vcc	-0.3 ～ 6.5		V
Power dissipation	Pd	DIP8	800(※1)	mW
		SOP8(F,RF)	450(※2)	
		SOP-J8(FJ,RFJ)	450(※3)	
		SSOP-B8(FV,RFV)	300(※4)	
		MSOP8(RFVM)	310(※5)	
Storage Temperature	Tstg	-65 ～ 125		°C
Operating Temperature	Topr	-40 ～ 85		°C
Terminal Voltage	—	-0.3 ～ Vcc+0.3		V

※1 Degradation is done at 8.0mW/°C for operation above Ta=25°C
※2 Degradation is done at 4.5mW/°C for operation above Ta=25°C
※3 Degradation is done at 4.5mW/°C for operation above Ta=25°C
※4 Degradation is done at 3.0mW/°C for operation above Ta=25°C
※5 Degradation is done at 3.1mW/°C for operation above Ta=25°C

◇RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	1.8 ～ 5.5	V
Input Voltage	Vin	0 ～ Vcc	

◇ELECTORICAL CHARACTERISTICS

Unless otherwise specified(Ta=-40～85℃,Vcc=2.5～5.5V)

Parameter	Symbol	Limit			Unit	Condition	Test Circuit
		Min.	Typ.	Max.			
Input Voltage "L" 1	VIL1	-0.3	—	0.8	V	4.0≦Vcc≦5.5	
Input Voltage "L" 2	VIL2	-0.3	—	0.2x Vcc	V	Vcc≦4.0	
Input Voltage "H" 1	VIH1	2.0	—	Vcc +0.3	V	4.0≦Vcc≦5.5	
Input Voltage "H" 2	VIH2	0.7x Vcc	—	Vcc +0.3	V	Vcc≦4.0	
Output Voltage "L" 1	VOL1	0	—	0.4	V	IOL=2.1mA, 4.0≦Vcc≦5.5	Fig.-4
Output Voltage "L" 2	VOL2	0	—	0.2	V	IOL=100μA	Fig.-4
Output Voltage "H" 1	VOH1	2.4	—	Vcc	V	IOH=-0.4mA, 4.0≦Vcc≦5.5	Fig.-5
Output Voltage "H" 2	VOH2	Vcc -0.2	—	Vcc	V	IOH=-100μA	Fig.-5
Input Leak Current	ILI	-1	—	1	μA	VIN=0～Vcc	Fig.-6
Output Leak Current	ILO	-1	—	1	μA	VOUT=0～Vcc, CS=0V	Fig.-7
Operating Current	ICC1	—	—	3.0	mA	fSK=2MHz, tE/W=5ms (WRITE)	Fig.-8
	ICC2	—	—	1.5	mA	fSK=2MHz (READ)	Fig.-8
	ICC3	—	—	4.5	mA	fSK=2MHz,tE/W=5ms (WRAL,ERAL)	Fig.-8
Standby Current	ISB	—	—	2	μA	CS=0V ,DO=OPEN	Fig.-9

Unless otherwise specified (Ta=-40～85℃,Vcc=1.8～2.5V)

Parameter	Symbol	Limit			Unit	Condition	Test Circuit
		Min.	Typ.	Max.			
Input Voltage "L"	VIL	-0.3	—	0.2x Vcc	V		
Input Voltage "H"	VIH	0.7x Vcc	—	Vcc +0.3	V		
Output Voltage "L"	VOL	0	—	0.2	V	IOL=100μA	Fig.-4
Output Voltage "H"	VOH	Vcc -0.2	—	Vcc	V	IOH=-100μA	Fig.-5
Input Leak Current	ILI	-1	—	1	μA	VIN=0～Vcc	Fig.-6
Output Leak Current	ILO	-1	—	1	μA	VOUT=0～Vcc, CS=0V	Fig.-7
Operating Current	ICC1	—	—	1.5	mA	fSK=500kHz,tE/W=5ms (WRITE)	Fig.-8
	ICC2	—	—	0.5	mA	fSK=500kHz (READ)	Fig.-8
	ICC3	—	—	2	mA	fSK=500kHz (WRAL,ERAL)	Fig.-8
Standby Current	ISB	—	—	2	μA	CS=0V, DO=OPEN	Fig.-9

○This product is not designed for protection against radioactive rays.

◇MEMORY CELL CHARACTERISTICS (Ta=25℃、Vcc=1.8～5.5V)

Parameter	Limit			Unit
	Min.	Typ.	Max.	
Write/Erase Cycle ※1	1,000,000	—	—	cycle
Data Retention ※1	40	—	—	year

※1:Not 100% Tested

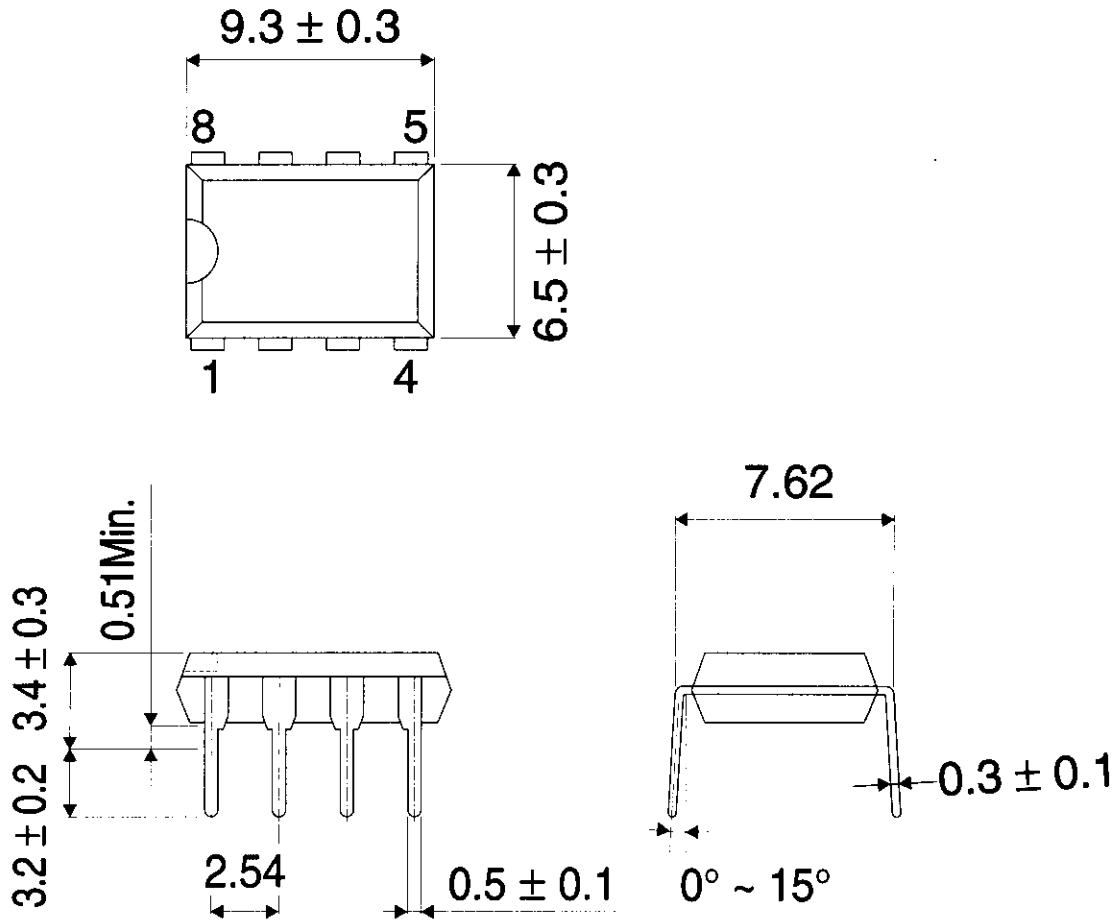


Fig.1-1 Outline Dimensions DIP8(BR93L66-W)

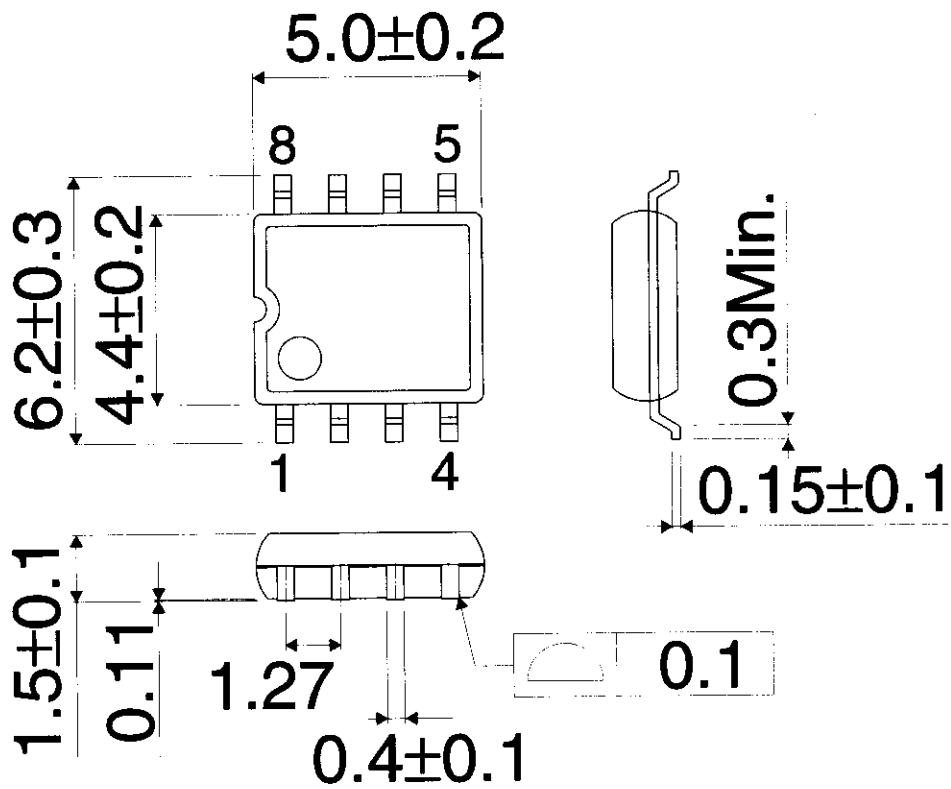


Fig.1-2 Outline Dimensions SOP8(BR93L66F-W)

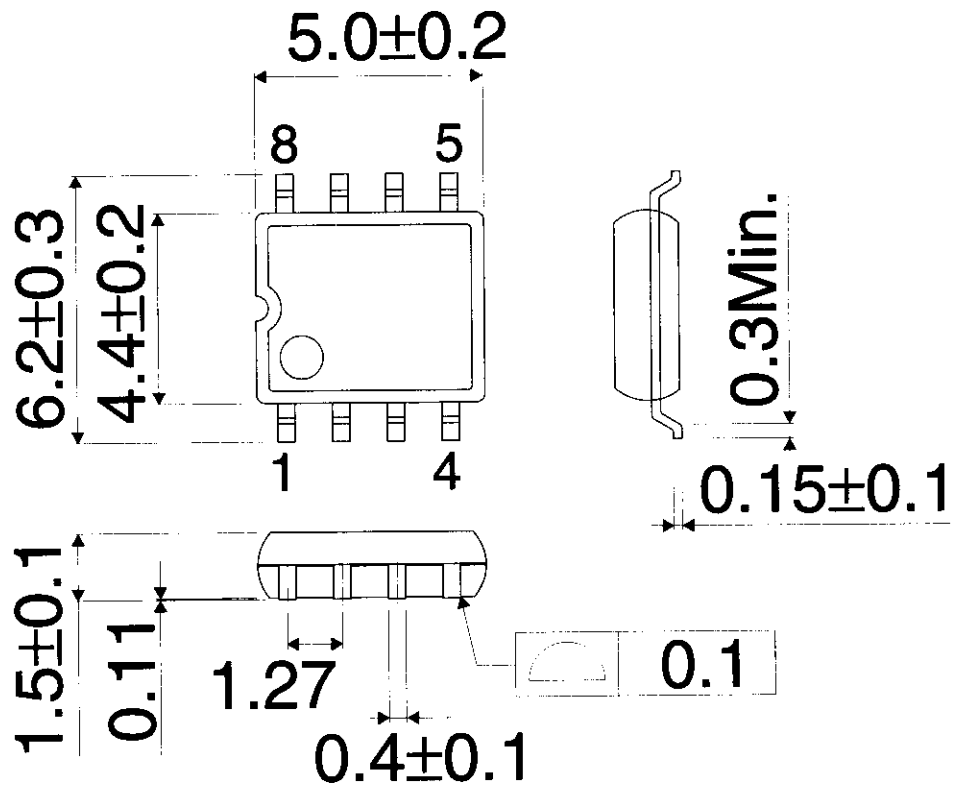


Fig.1-3 Outline Dimensions SOP8(BR93L66RF-W)

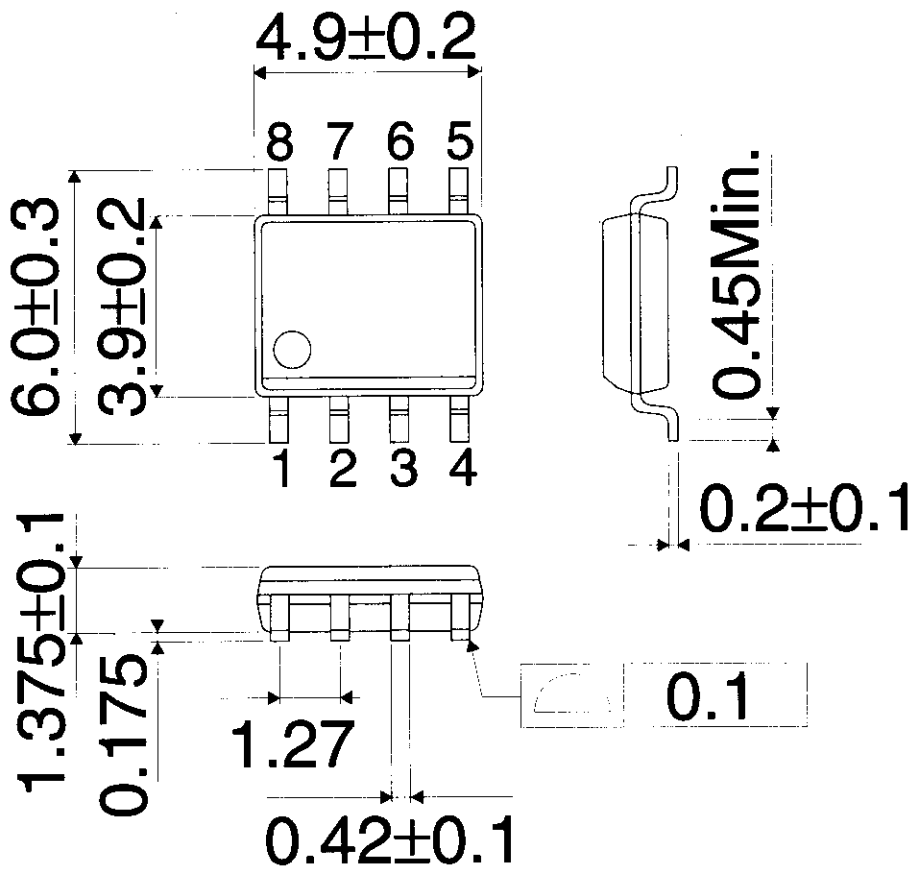


Fig.1-4 Outline Dimensions SOP-J8(BR93L66FJ-W)

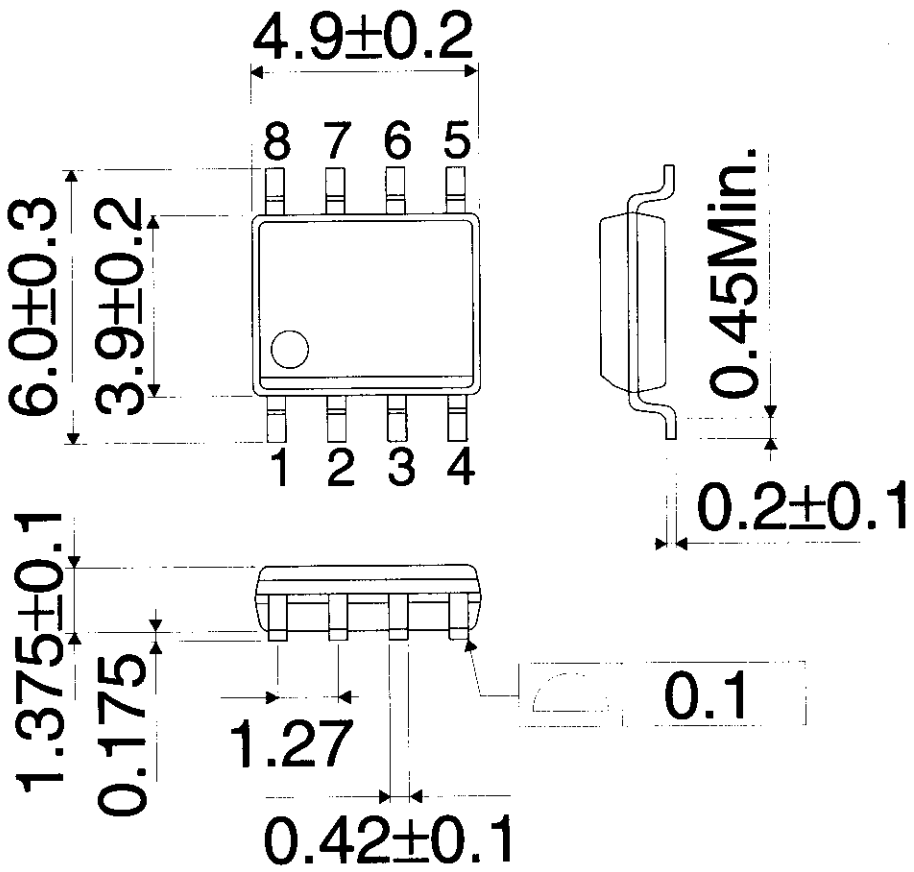


Fig.1-5 Outline Dimensions SOP-J8(BR93L66RFJ-W)

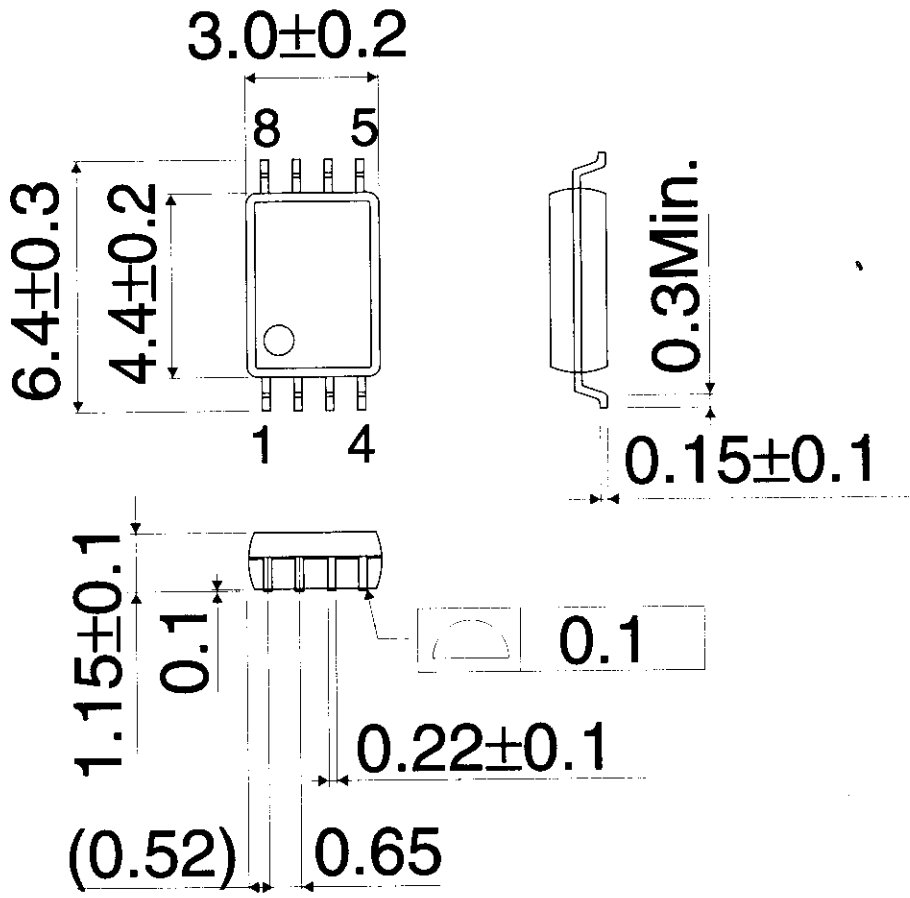


Fig.1-6 Outline Dimensions SSOP-B8(BR93L66FV-W)

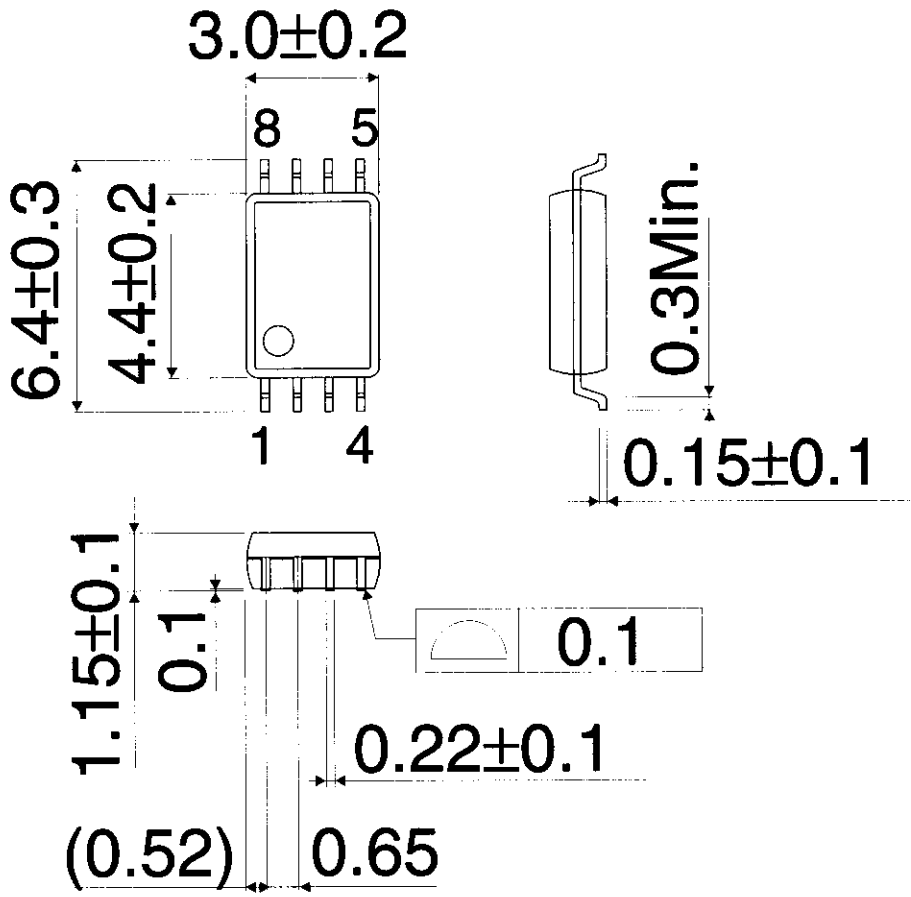


Fig.1-7 Outline Dimensions SSOP-B8(BR93L66RFV-W)

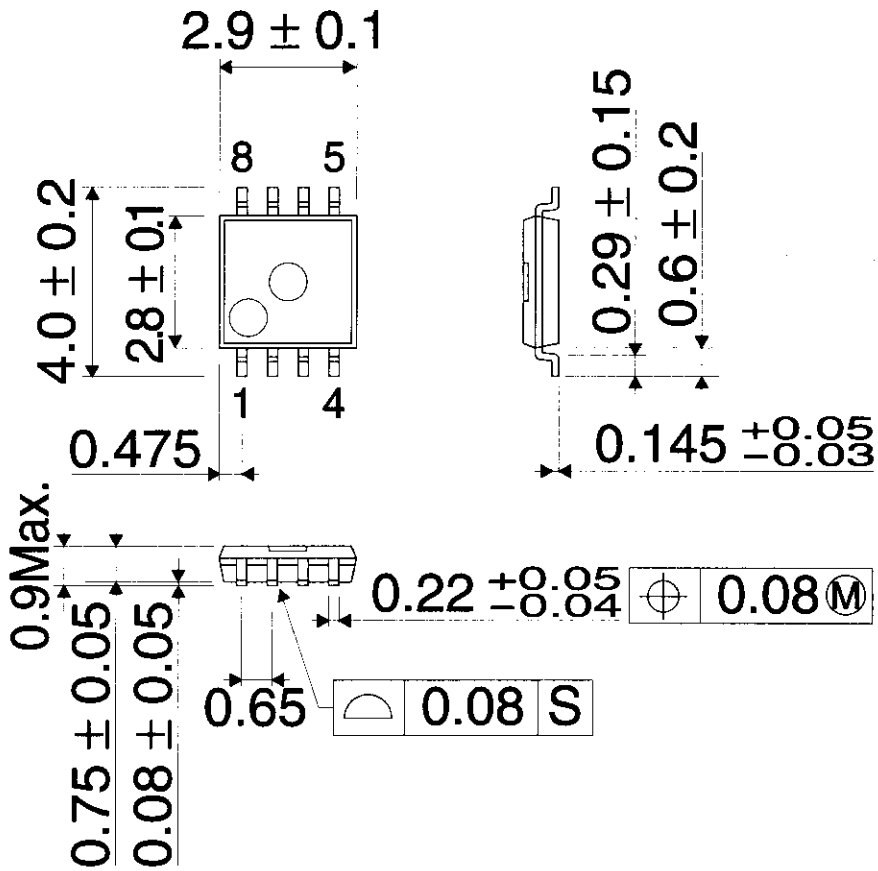


Fig.1-8 Outline Dimensions MSOP8(BR93L66RFVM-W)

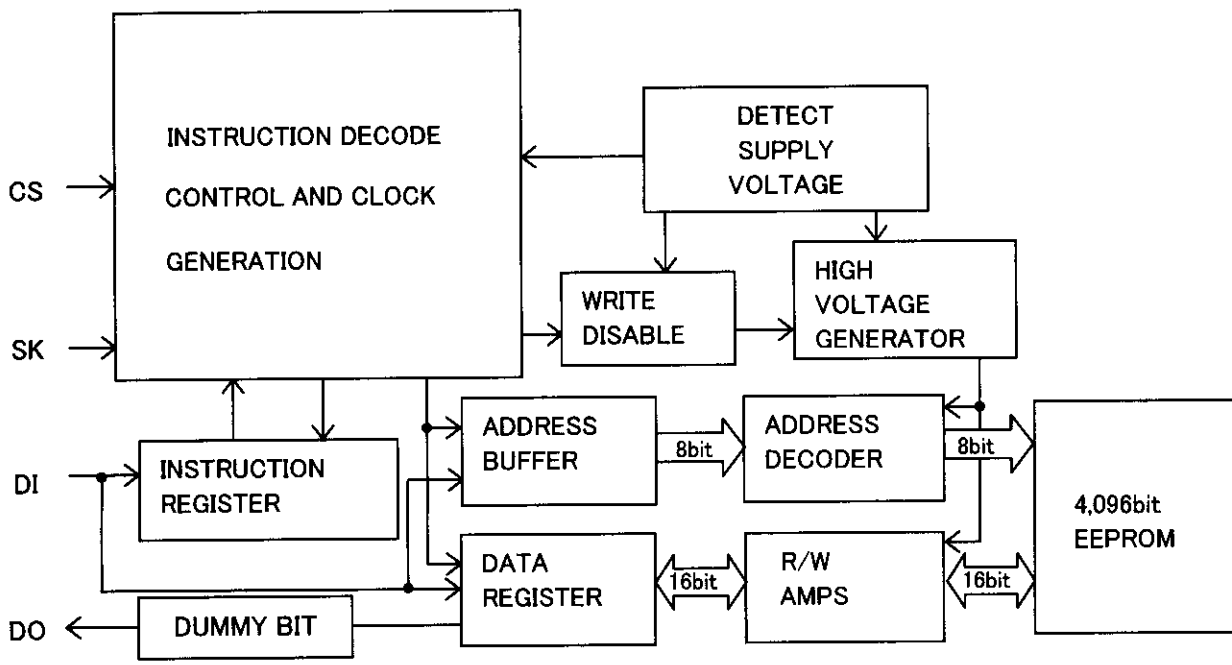


Fig.-2 Block Diagram

◇PIN CONFIGURATIONS

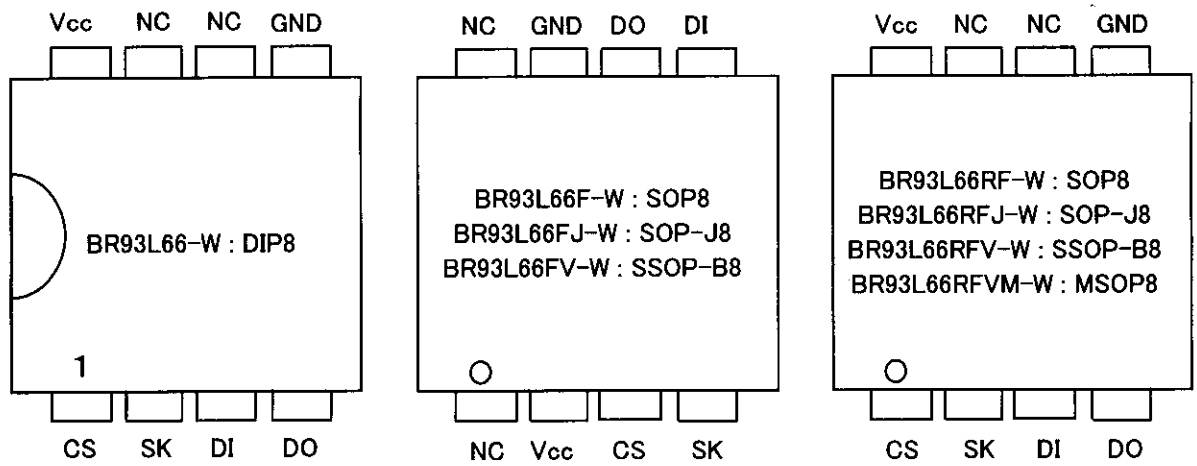
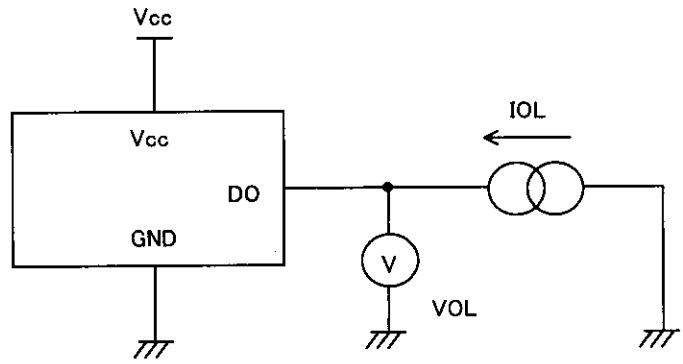


Fig.-3 Pin Configurations

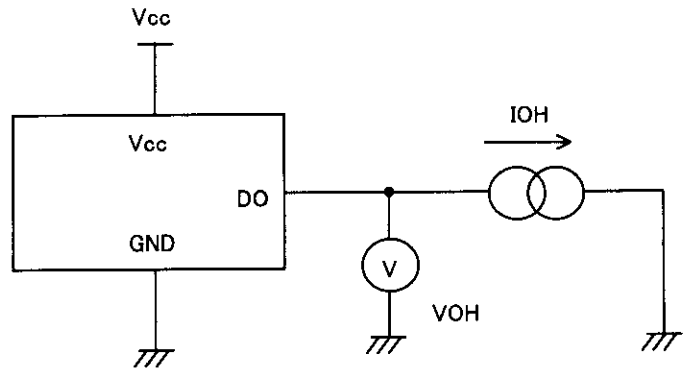
◇TERMINAL FUNCTION

Terminal	IN/OUT	Function
Vcc	—	Power Supply
GND	—	Ground (0V)
CS	INPUT	Chip Select Control
SK	INPUT	Serial Data Clock Input
DI	INPUT	Start Bit, Op. code, Address, Serial Data Input
DO	OUTPUT	Serial Data Output , Ready/$\overline{\text{Busy}}$ Status Output
NC	—	No Connection (Vcc or GND or OPEN)

◇TEST CIRCUIT



Control Output Pin to "L"
Fig.-4 Output Low Voltage Test Circuit



Control Output Pin to "H"
Fig.-5 Output High Voltage Test Circuit

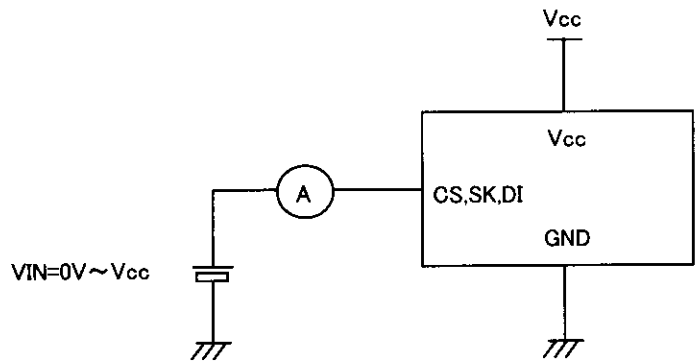


Fig.-6 Input Leakage Current Test Circuit

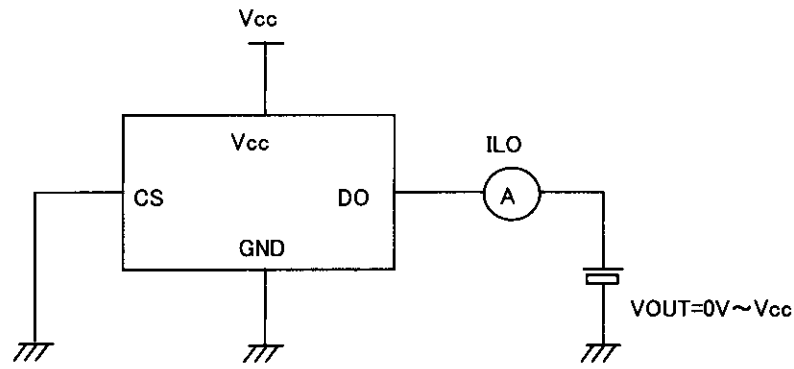


Fig.-7 Output Leakage Current Test Circuit

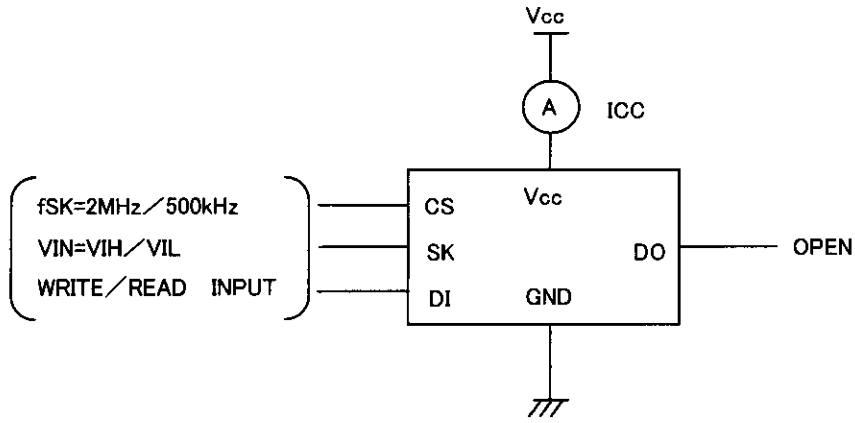


Fig.-8 Operating Current Test Circuit

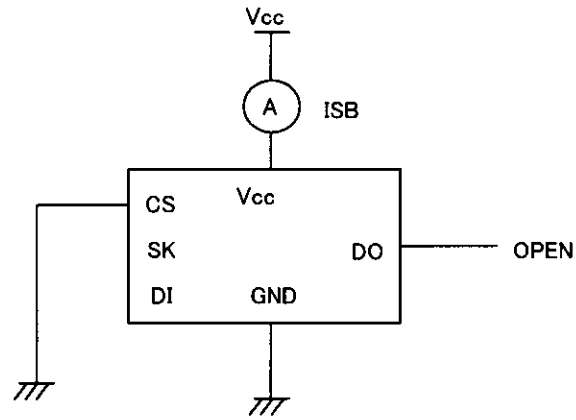


Fig.-9 Standby Current Test Circuit

◇SYNCHRONOUS DATA TIMING

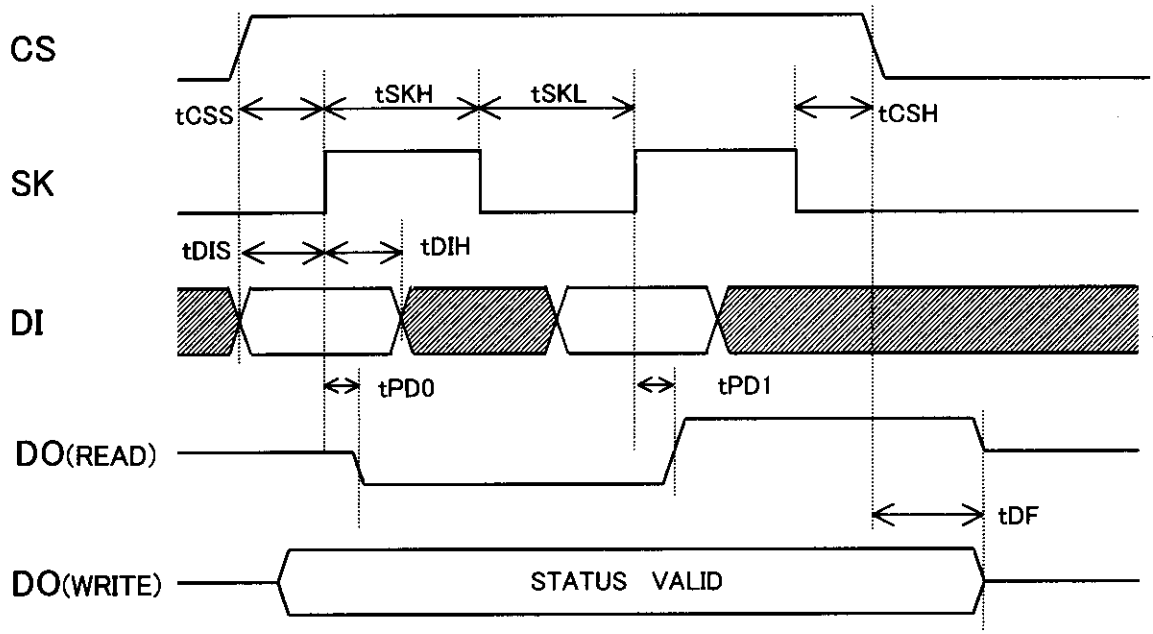


Fig.-10 Synchronous data timing

○Input Data are clocked in from DI pin at the rising edge of the clock (SK).

○Output data from DO pin toggles at the rising edge of the clock(SK) during read mode.

○When CS is brought "H" after the write command , STATUS signal (Ready/$\overline{\text{Busy}}$) becomes active on DO pin till the start bit of next command.
STATUS signal is active during CS is high, and DO pin outputs High-Z when CS is low.

○For internal reset , CS must be brought "L" after any commands.

◇AC OPERATING CHARACTERISTICS(Ta=-40~85℃、Vcc=2.5~5.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SK Clock Frequency	fSK	-	-	2	MHz
SK High Time	tSKH	230	-	-	ns
SK Low Time	tSKL	230	-	-	ns
CS Low Time	tCS	200	-	-	ns
CS Setup Time	tCSS	50	-	-	ns
DI Setup Time	tDIS	100	-	-	ns
CS Hold Time	tCSH	0	-	-	ns
DI Hold Time	tDIH	100	-	-	ns
Data "1" Output Delay Time	tPD1	-	-	200	ns
Data "0" Output Delay Time	tPD0	-	-	200	ns
CS to Status Valid	tSV	-	-	150	ns
CS to Output High-Z	tDF	-	-	150	ns
Write Cycle time	tE/W	-	-	5	ms

◇AC OPERATING CHARACTERISTICS(Ta=-40～85℃、Vcc=1.8～2.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SK Clock Frequency	fSK	-	-	500	kHz
SK High Time	tSKH	0.8	-	-	μs
SK Low Time	tSKL	0.8	-	-	μs
CS Low Time	tCS	1	-	-	μs
CS Setup Time	tCSS	200	-	-	ns
DI Setup Time	tDIS	100	-	-	ns
CS Hold Time	tCSH	0	-	-	ns
DI Hold Time	tDIH	100	-	-	ns
Data "1" Output Delay Time	tPD1	-	-	0.7	μs
Data "0" Output Delay Time	tPD0	-	-	0.7	μs
CS to Status Valid	tSV	-	-	0.7	μs
CS to Output High-Z	tDF	-	-	200	ns
Write Cycle time	tE/W	-	-	5	ms

◇INSTRUCTION CODE

Instruction	Start Bit	Op Code	Address	Data
Read (*1)	1	10	A7,A6,A5,A4,A3,A2,A1,A0	D15~D0 (READ DATA)
Write Enable (WEN)	1	00	1 1 * * * * * *	
Write (*2)	1	01	A7,A6,A5,A4,A3,A2,A1,A0	D15~D0 (WRITE DATA)
Write All (WRAL) (*2)	1	00	0 1 * * * * * *	D15~D0 (WRITE DATA)
Write Disable (WDS)	1	00	0 0 * * * * * *	
Erase	1	11	A7,A6,A5,A4,A3,A2,A1,A0	
Erase All (ERAL)	1	00	1 0 * * * * * *	

・Address and data must be transferred from MSB.
・"*" Means either VIH or VIL

※START BIT

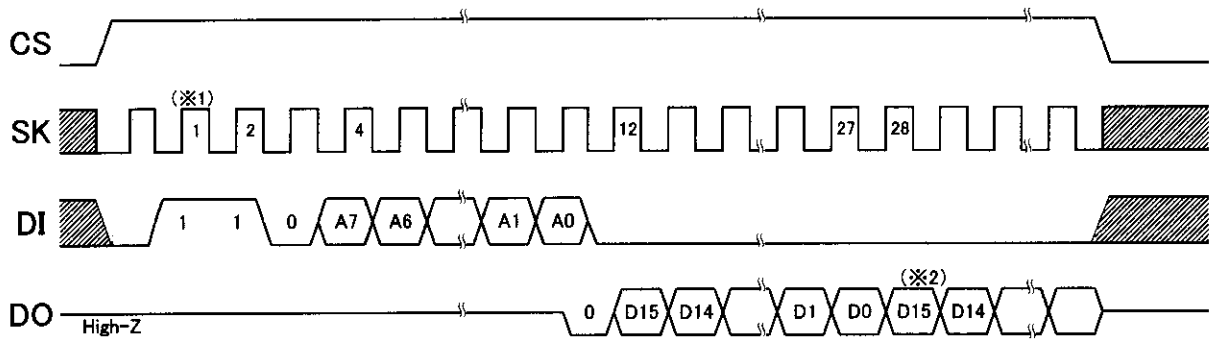
Start Bit means a logical "1" input after CS goes high.
This start bit proceeds beginning of all instructions.

(*1) : After one Read instruction segment is received, when CS remains High , the address pointer automatically cycles to the next higher register address, giving a continuous string of output data, depending on the device and the starting address.

(*2) : The previous data in the address locations are automatically erased and written the desired data, when "Write" or "Write All" instruction is received. No erase command is needed.

◇TIMING CHART

1.READ CYCLE TIMING



(※2) next Address
(Auto-increment)

Fig.-11 Read Cycle Timing

(※1) Start bit

This device recognizes the first data "1" after CS goes high as a start bit. You can input plenty of "0" before "1", still the data "1" works as a start bit.

○The addressed 16 bit of data are clocked out after "Read" instruction is received. During the 11th clock is high, the device output "0" (dummy 0) as a sign of data output start.
This device has the auto-increment feature that provides the whole data of the memory array with one read command.
Just keep CS high and SK clocking, the device outputs the next address data following the addressed 16 bits of data, please.

2.WRITE ENABLE CYCLE TIMING

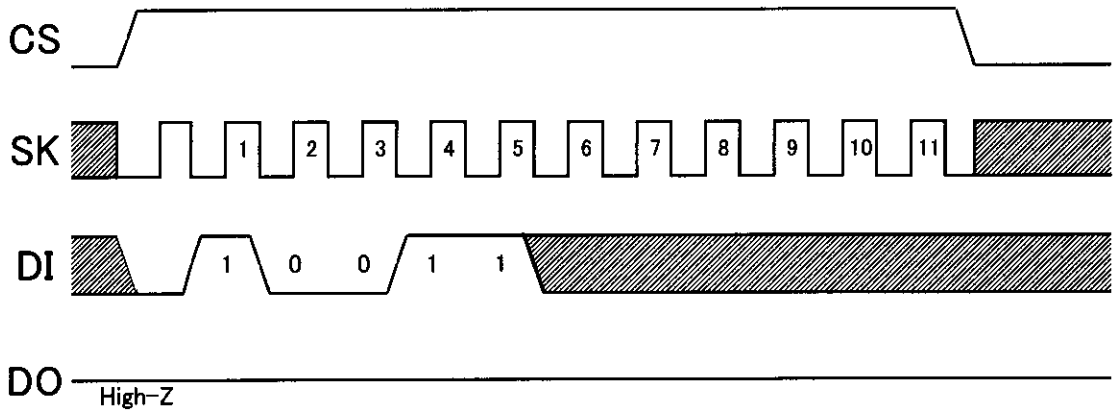


Fig.-12 Write Enable Cycle Timing

○After the power is on, the device is in the disable mode.
This "Write Enable" instruction must be proceeded before the any write commands.
After "Write Enable" is executed, the device becomes in the enable mode.
This enable mode is valid until the power is off or the device receives "Write Disable" instruction.
Neither the "Write Enable" nor the "Write Disable" instruction has any effect on the "Read" instruction. This device does not matter the state ("H" or "L") of DI after the 6th clock of SK. Please keep inputting six more SK signals.

3. WRITE CYCLE TIMING

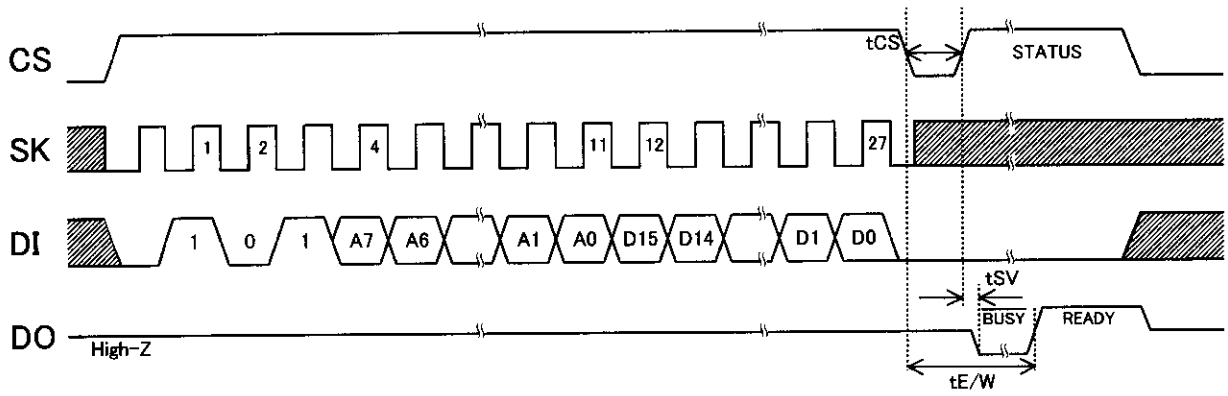


Fig.-13 Write Cycle Timing

○This "Write" command writes 16 bits of data into the specified address.
The falling edge of CS after the 27th clock initiates high voltage cycle, which writes the data into non-volatile memory array.
Ready/$\overline{\text{Busy}}$ signal indicates this high voltage cycle from DO pin. During this high voltage cycle (busy state), the device does not receive any command.

4.WRITE ALL CYCLE TIMING

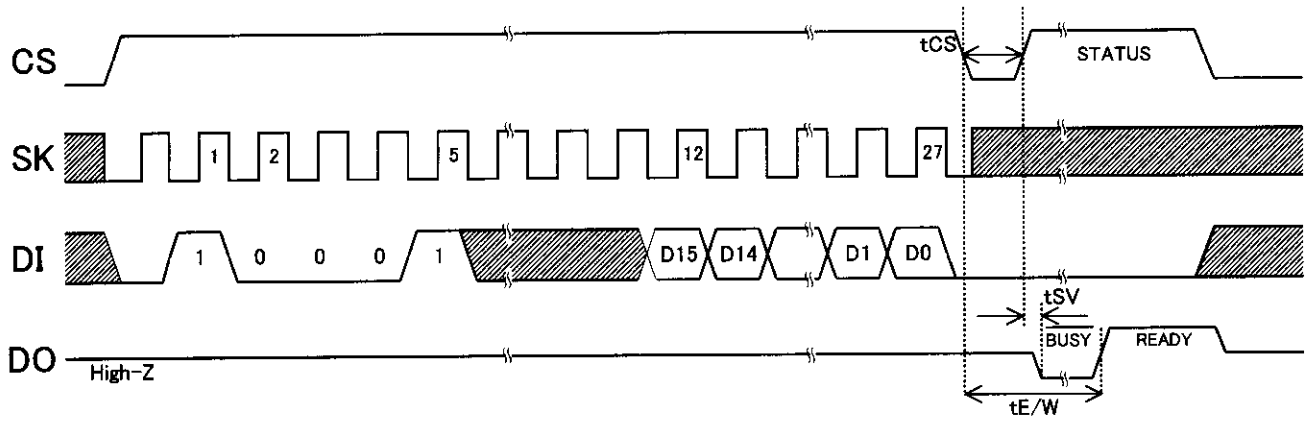


Fig.-14 Write All Cycle Timing

○This command writes 16 bits of data into the all address.
It takes maximum 5ms, because all the data are written in to memory array at the same time.

5.WRITE DISABLE CYCLE TIMING

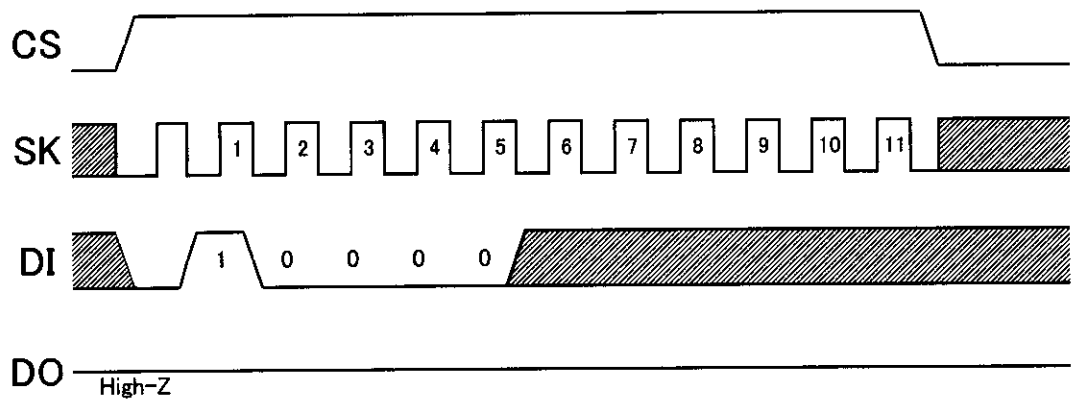


Fig.-15 Write Disable Cycle Timing

○This command put the device into the disable mode.
After the power on, the device is also in the disable mode.
The "Read" command can be proceeded even in the disable mode.
We recommend this "Write Disable" command execution after any write commands in order to prevent inadvertent write. This device does not matter the state ("H" or "L") of DI after the 6th clock of SK. Please keep inputting six more SK signals.

6.ERASE CYCLE TIMING

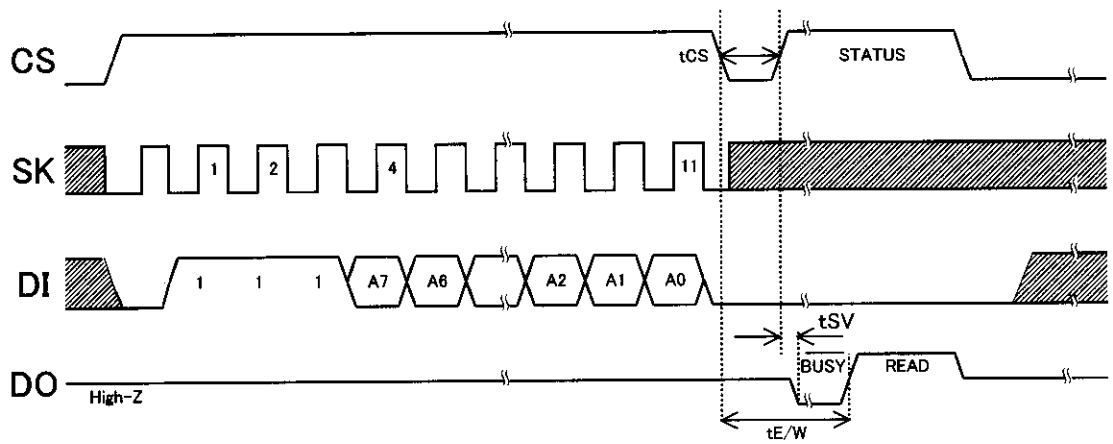


Fig.-16 Erase Cycle Timing

○This "Erase" command writes all bits in the specified address to "1".
The falling edge of CS after the 11th clock initiates high voltage cycle, which writes the data into non-volatile memory array.
The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device.

7. ERASE ALL CYCLE TIMING (ERAL)

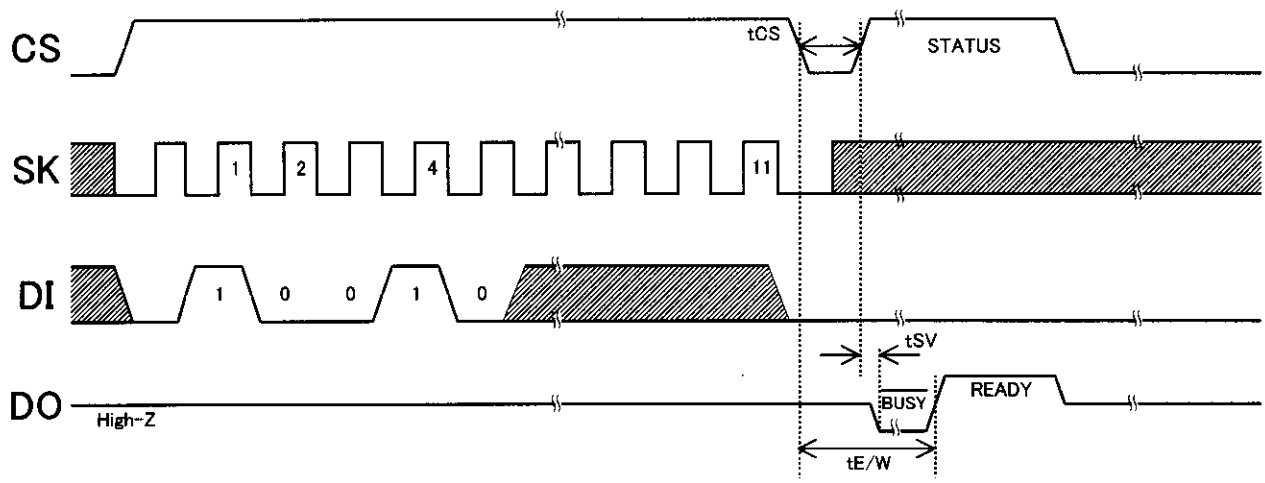


Fig.-17 Erase All Cycle Timing

○This "Erase All" command writes all bits in the all address to "1".
The falling edge of CS after the 11th clock initiates high voltage cycle, which writes the data into non-volatile memory array.
The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device.

◇READY/$\overline{\text{BUSY}}$ Status (DO pin)

After the write commands input, CS goes low to initiate high voltage cycle and goes high again. Then Ready/$\overline{\text{Busy}}$ signal will be shown on the DO pin.

R/$\overline{\text{B}}$ = Low : under writing
After spending tE/W (Max. 5ms) operating the internal timer, the device automatically finishes writing.
During tE/W, the memory array is accessed and any instruction is not received.

R/$\overline{\text{B}}$ = High : ready
Auto programming has been completed. The device is ready to receive the next instruction without waiting tE/W. In this case, keep DI="L" during CS is High.

※ During this high voltage cycle (busy state), the device does not receive any command. During the device is ready to next receive command (ready state), it is possible to make malfunction or inadvertent write when the device receives any signals.

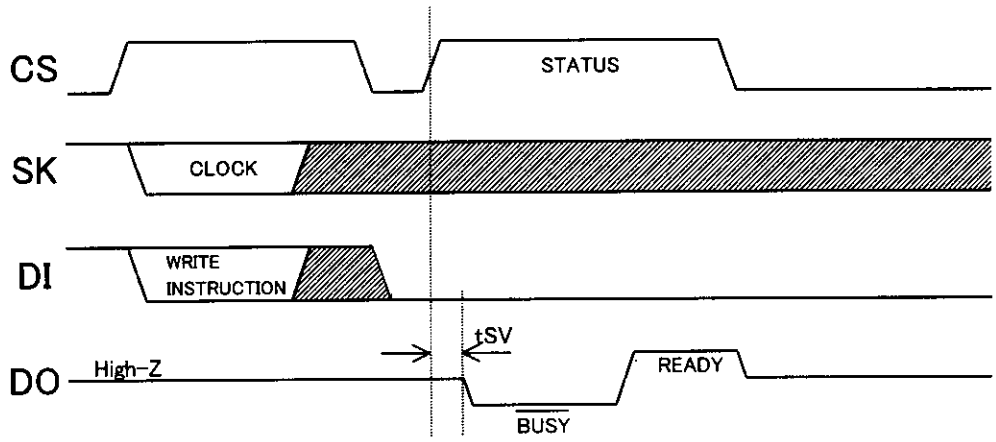


Fig.-18 READY/$\overline{\text{BUSY}}$ Status Output Timing

This product described in this specification is a strategic product and/or subject to COCOM regulations. It should not be exported without authorization from the appropriate Government authorities.

Application Note

<Contents>

1)COMMAND CANCEL

○READ

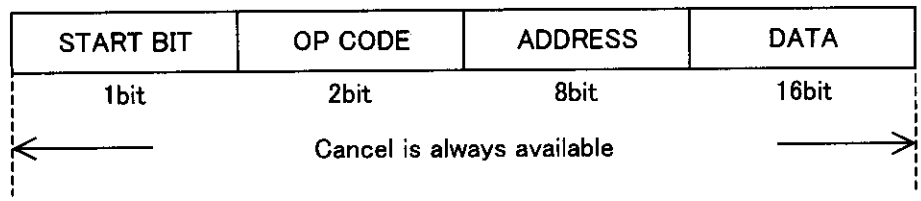


Fig.1-1 READ CANCEL EFFECTIVE TIMING

・Method of cancel : CS="L"

○WRITE, WRAL(Write All)

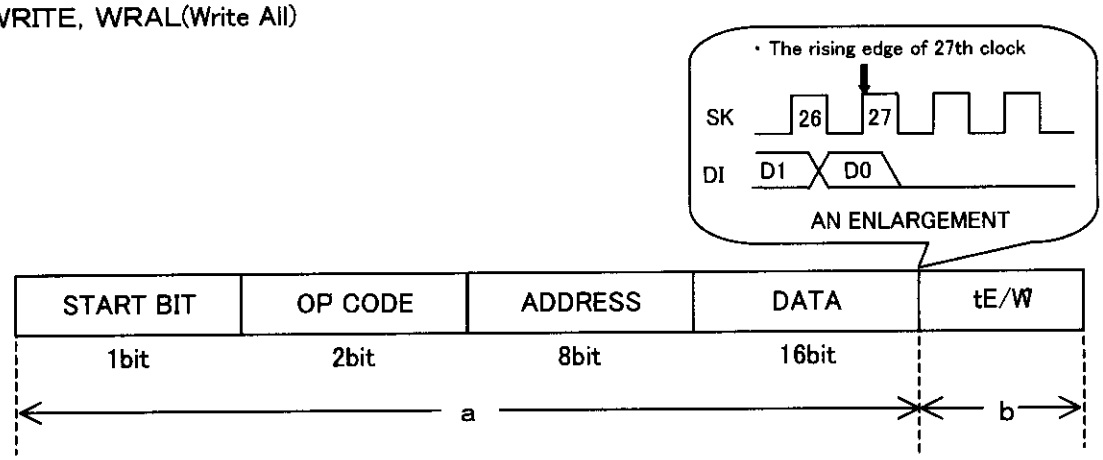


Fig.1-2 WRITE AND WRAL CANCEL EFFECTIVE TIMING

a : The period from start bit to the rising edge of 27th clock
CS = "L" cancels these commands.

b : The Period from the rising edge of 27th clock to the end of internal write cycle (tE/W)
There is no way to cancel this command.
If power is down during this period, the data is not guaranteed, so that write correct data again please.
It is impossible to cancel this command by sending additional SK clock signal.

○ERASE, ERAL(Erase All)

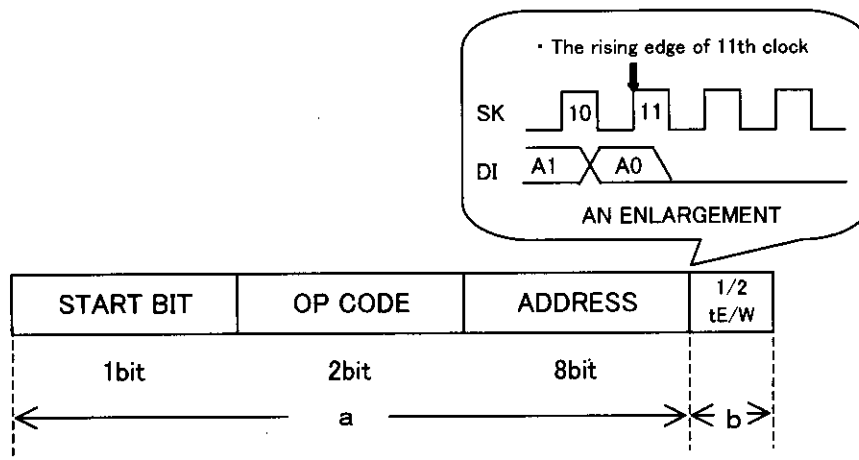


Fig.1-3 ERASE AND ERAL EFFECTIVE TIMING

a : The period from start bit to the rising edge of 11th clock
CS = "L" cancels these commands.

b : The period from the rising edge of 11th clock to the end of internal write cycle (tE/W)
There is no way to cancel this command.
If power is down during this period, the data is not guaranteed, so that write correct data again please.
It is impossible to cancel this command by sending additional SK clock signal.

2) STAND BY

○STANDBY CURRENT

CS="L" makes standby current constant. SK and DI states do not affect it.

○TIMING (Start Bit)

Data may be inputted if CS is brought high when SK="H" states, as shown Fig.2-1.(See Fig.2-1)
Please keep SK and DI input signals "L", if CS is brought high during stand by and power ON/OFF. (See Fig.2-2)

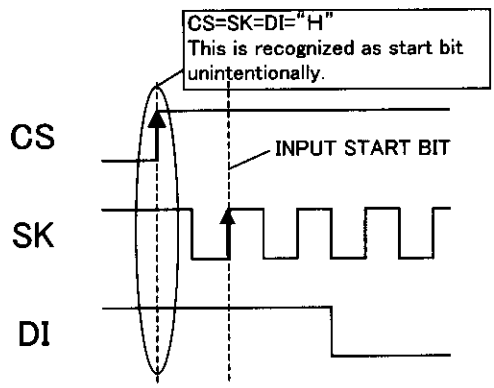


Fig.2-1 NOT PROPOSED TIMING

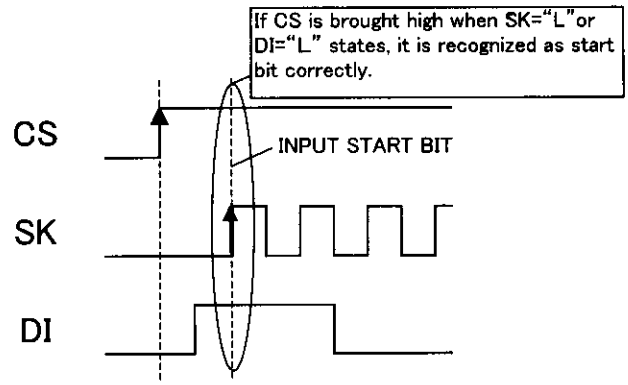


Fig.2-2 PROPER TIMING

3)POWER ON/OFF

・Please keep CS "L" during power ON/OFF.

The device is an active state during CS is high. The extraordinary function or data collaption may occur because of noise etc., if power-up is done with CS "H". In order to prevent above errors from happening, keep CS "L" during power ON. (The device does not receive any command during CS is low.)

It may continue at low Vcc by capacitance of Vcc line during power off. Please keep CS "L" during power off because of the device may make malfunction and inadvertent write.

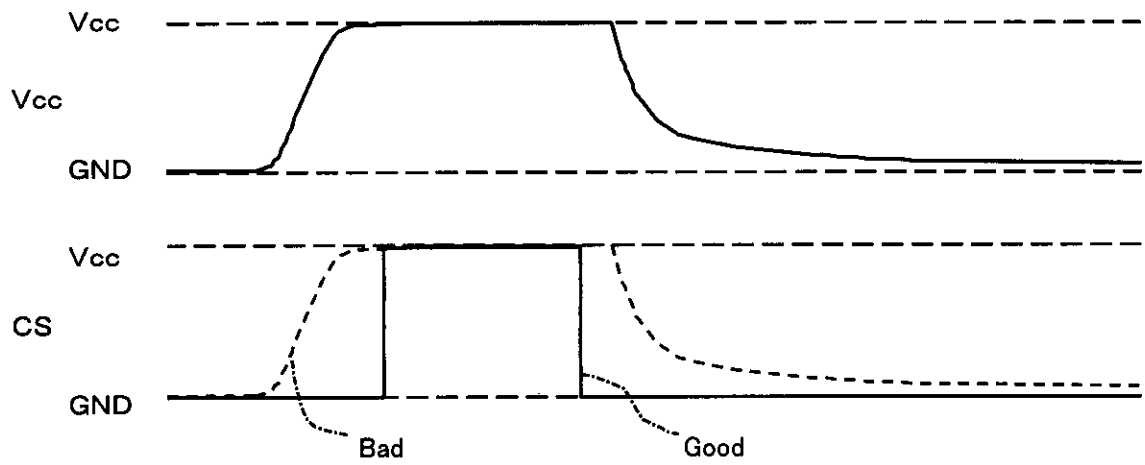


Fig.3-1 CS TIMING DURING POWER ON/OFF

(Bad example) CS follows Vcc. (CS is pull up to Vcc)

CS is always high in this case the noise may force the device to malfunction and inadvertent write.
※It may occur even if CS is High-Z.

(Good example) CS is low during power ON/OFF.

Please take more than 10ms between power ON and power OFF, or the internal circuit is not always reset.

OP.O.R. CIRCUIT

In order to prevent an inadvertent write, the device has the feature of P.O.R..
After the power is on, the device is in the write disable mode. P.O.R. works only during power up.
The noise may force the device to make the write enable mode with CS="H" during power ON/OFF.
In the case of power up, keep the following conditions to ensure function of P.O.R.

1. It is necessary to be CS "L"
2. Follow the recommended conditions of tR, tOFF, Vbot for the function of P.O.R. during power up.

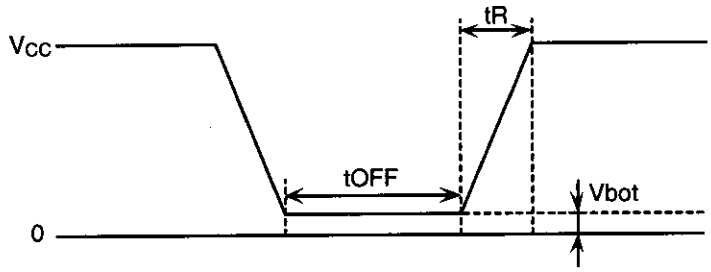


Fig.3-2 Vcc wave form

Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

OLVCC CIRCUIT

LVCC (Vcc-Lock out) circuit inhibits write operation at low voltage, and prevents an inadvertent write.
When Vcc is below the LVCC voltage (Typ.=1.2V), write operation is inhibited.

4) NOISE

○NOISE ON Vcc (about bypass capacitor)

Noise and surges on power line may cause the abnormal function. It is recommended that the bypass capacitor (0.1 μF) are attached on the Vcc and GND line beside the device.
The attachment of bypass capacitor on the board near by connector is recommended.

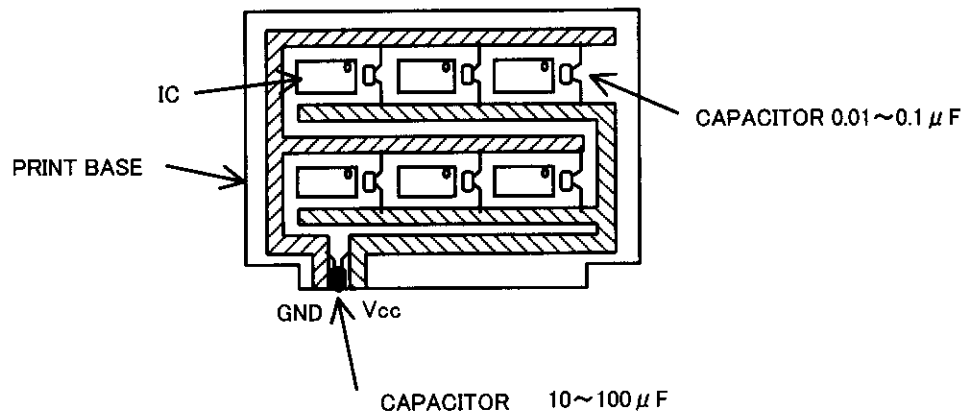


Fig.4 NOISE ON Vcc COUNTERMEASURE EXAMPLE

○NOISE ON SK

If SK line has a lot of noise and rising time of SK is long, the device may recognize noise as a clock. Therefore this device has a schmitt trigger (about 0.2V) on SK pin. However to get rid of noise, less than 100ns of SK rising time(tR) is recommended. If SK rising time is more than 100ns, pay attention to reduce the noise, please.
Please keep rising time and falling time as short as possible to ensure data transfer reliability.

5) INPUT/OUTPUT PIN EQUIVALENT CIRCUIT

○OUTPUT CIRCUIT

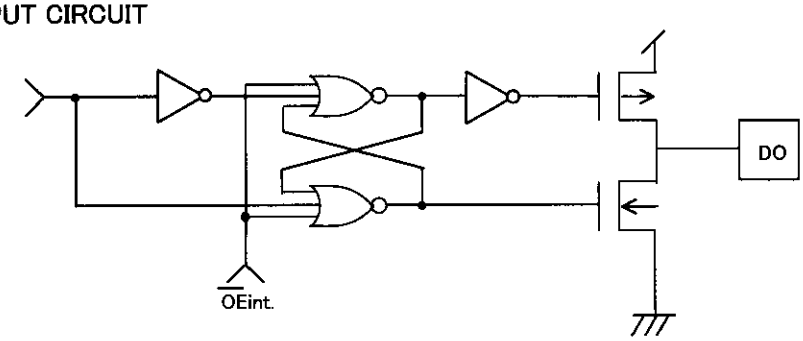


Fig.5-1 DO PIN EQUIVALENT CIRCUIT

○INPUT CIRCUIT

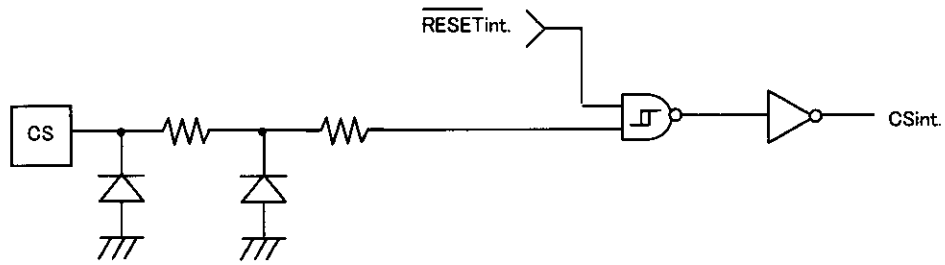


Fig.5-2 CS PIN EQUIVALENT CIRCUIT

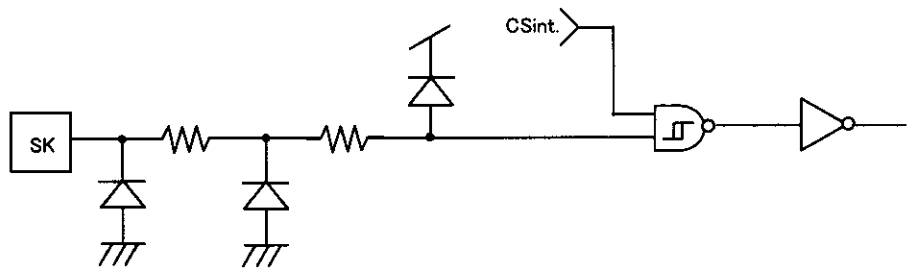


Fig.5-3 SK PIN EQUIVALENT CIRCUIT

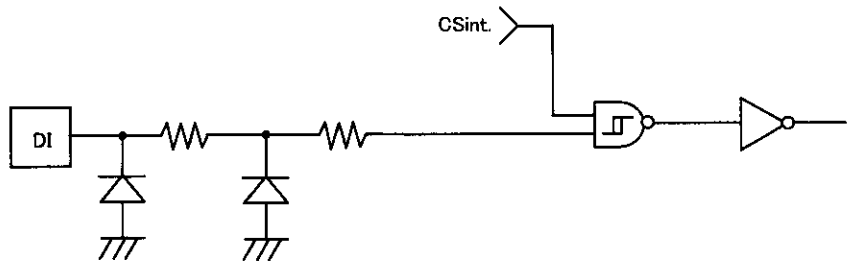


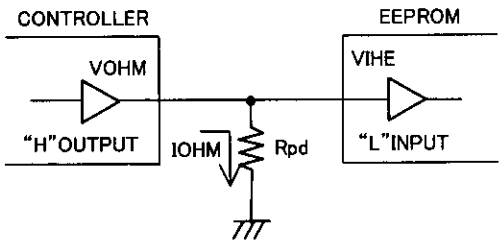
Fig.5-4 DI PIN EQUIVALENT CIRCUIT

6)I/O APPLICATION CIRCUIT

1. Pull down resister is recommended.
   When CS is "L" during power ON/OFF, error operating and writing is protected.

○ PULL DOWN RESISTER OF CS PIN

The pull down resister is needed in order to prevent error operating and writing from happening. Decide the value of this resister (Rpd) properly, considering VOH, IOH characteristics of controller.



$$Rpd \geqq \frac{VOHM}{IOHM} \cdots ①$$

$$VOHM \geqq VIHE \cdots ②$$

Example) When Vcc=5V,VIHE=2V,VOHM=2.4V,IOHM=2mA ,
According to ①,

$$Rpd \geqq \frac{2.4}{2\times10^{-3}}$$

$$\therefore \quad Rpd \geqq 1.2[k\Omega]$$

If the Rpd is under the conditions of the equation ①,
VOHM is 2.4V or more.
If the Rpd is under the conditions of the equation ②,
VIHE(=2.0V) is VOHM or less.

- VIHE : VIH specification of EEPROM
- VOHM : VOH specification of CONTROLLER
- IOHM : IOH specification of CONTROLLER

Fig.6-1 PULL DOWN RESISTER OF CS PIN

2. DO may have either pull up and down.
   DO is "High-Z" except output data and R/$\overline{B}$ status timing. If the controller make malfunction with state "High-Z", it is needed the pull up or down resister to DO. If the state of DO pin do not affect it, the DO pin may be left "High-Z".
   In case that the DO pin is no connection, if CS, SK and DI is high during DO states ready, the device recognize it as a start bit and cancel state ready. DO looks "H" by the pull up resister of DO. (See Fig.6-2)

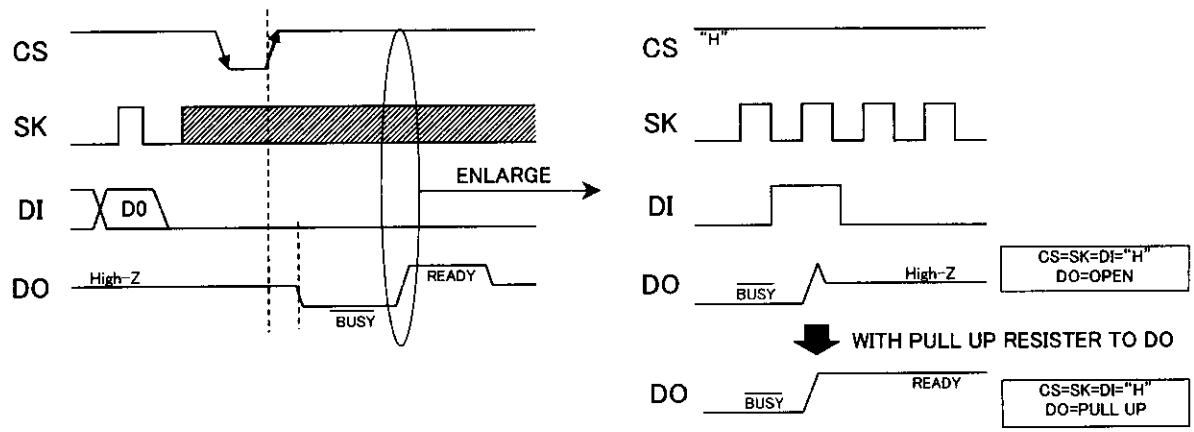


Fig.6-2 READY OUTPUT TIMING WHEN DO IS OPEN

OPULL UP/DOWN RESISTER OF DO PIN

Decide the value of this resister (Rpu) properly, by considering VIH, VIL characteristics of a controller, which control the device and VOH, IOH, VOL, IOL characteristics of the device.

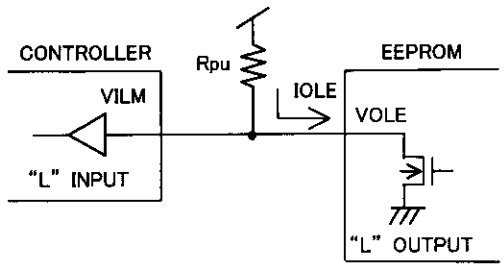


Fig.6-3 PULL UP RESISTER OF DO PIN

$$Rpu \geqq \frac{Vcc-VOLE}{IOLE} \quad \cdots ③$$

$$VOLE \leqq VILM \quad \cdots ④$$

Example) When Vcc=5V, VOLE=0.4V, IOLE=2.1mA, VILM=0.8V,
According to ③

$$Rpu \geqq \frac{5-0.4}{2.1 \times 10^{-3}}$$

$$\therefore \quad Rpu \geqq 2.2[k\Omega]$$

If the Rpu is under the conditions of the equation ③, VOLE is 0.4V or less.
If the Rpu is under the conditions of the equation ④, VILM(=0.8V) is VOLE or more.

- VOLE : VOL specification of EEPROM
- IOLE : IOL specification of EEPROM
- VILM : VIL specification of CONTROLLER

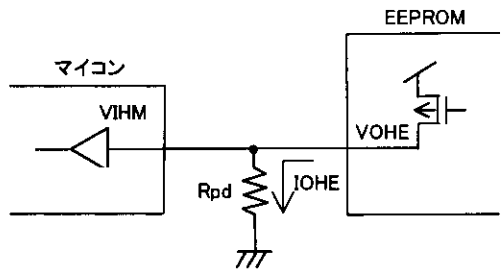


Fig.6-4 PULL DOWN RESISTER OF DO PIN

$$Rpd \geqq \frac{VOHE}{IOHE} \quad \cdots ⑤$$

$$VOHE \geqq VIHM \quad \cdots ⑥$$

Example) When Vcc=5V,VOHE=Vcc-0.2V,IOHE=0.1mA,
VIHM=Vcc × 0.7V, According to ⑤

$$Rpd \geqq \frac{5-0.2}{0.1 \times 10^{-3}}$$

$$\therefore \quad Rpd \geqq 48[k\Omega]$$

If the Rpu is under the conditions of the equation ⑤, VOHE is 2.4V or more.
If the Rpu is under the conditions of the equation ⑥, VIHM(=3.5V) is VOHE or less.

- VOHE : VOH specification of EEPROM
- IOHE : IOH specification of EEPROM
- VIHM : VIH specification of CONTROLLER

7) DI/O PORT (TO CONNECT DI AND DO)

The device has DI and DO (independent each other). But they can be connected, then controlled by signal DI/O port. (1 port)

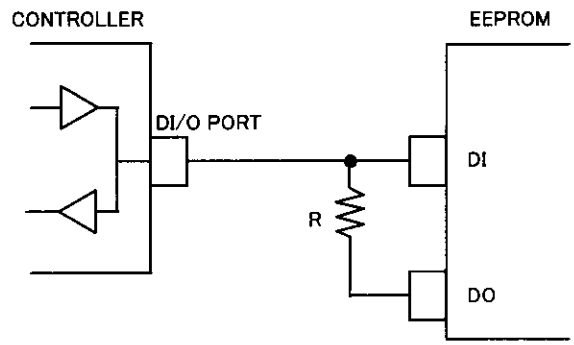


Fig.7-1 DI/O PORT TO CONNECT DI AND DO

○BUS CONNECTION BETWEEN CONTROLLER AND EEPROM (DO FEED BACK TO DI)

There are two timing that has bus conflict between DI/O output and DO.

(1) Half clock cycle for A0 (last address bit) in read mode. (See Fig.7-2)
DO outputs the dummy "0".
→There are bus contention when A0="1" are inputted.

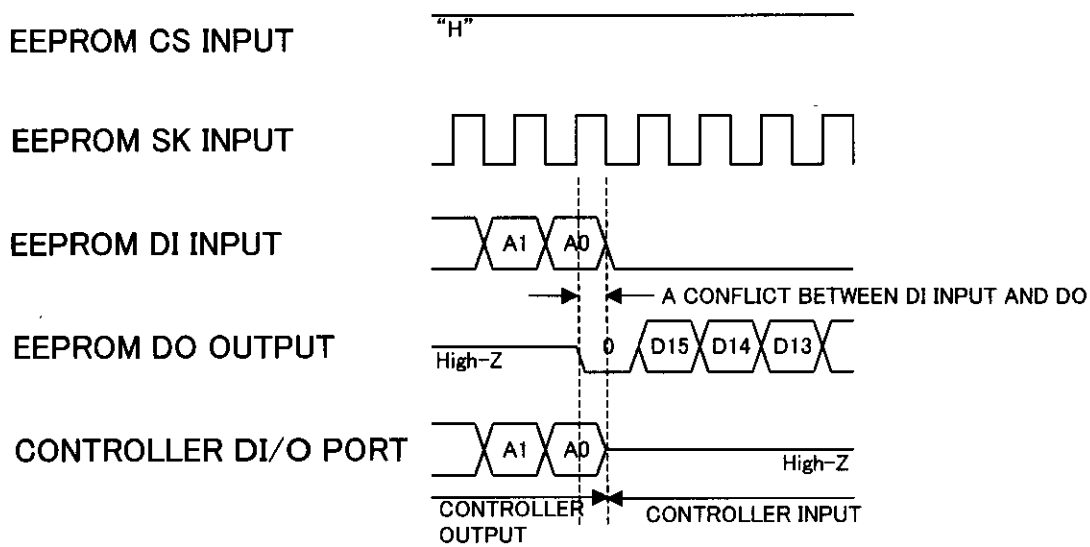


Fig.7-2 DI/O PORT TO CONNECT DI AND DO READ OPERATION

(2) CS="H" after program command. (See Fig.7-3)
DO outputs READY/$\overline{\text{BUSY}}$ signal, until start bit is inputted.
DO makes "High-Z" states by recognizing a start bit.
→When CS is brought high with controller output "L" from DI/O port during next command input, the device outputs ready signal from DO pin and makes a current overload.

In timing of (1), (2), to insert R between DI and DO will solve above problems.

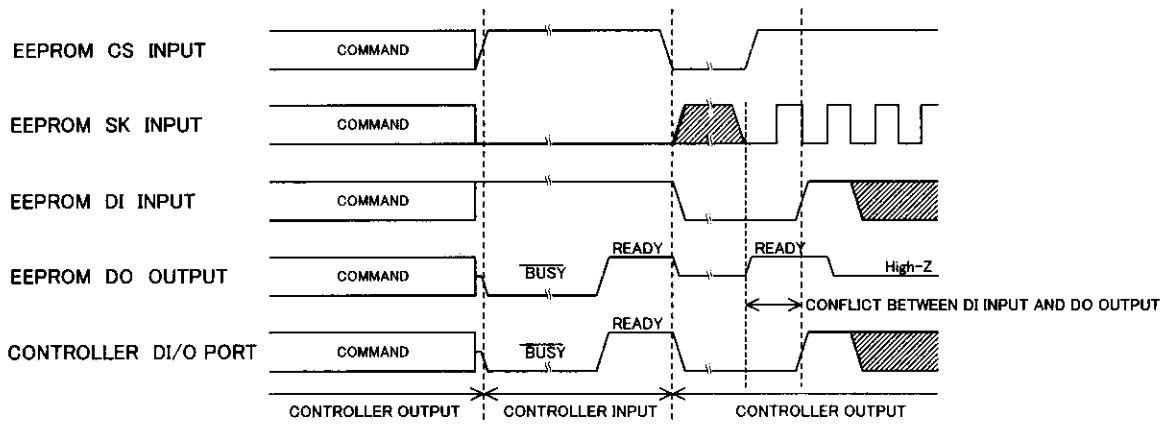
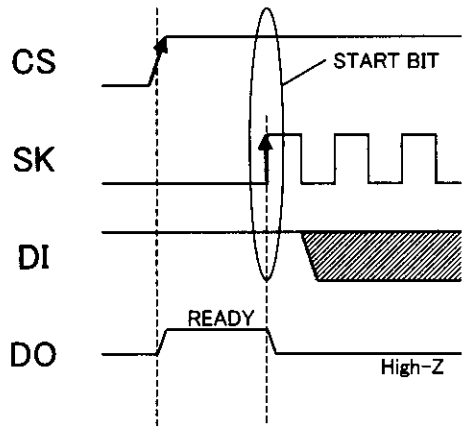


Fig.7-3 DI/O PORT TO CONNECT DI AND DO DURING WRITE OPERATION

NOTE) In the case of (2), pay attention to the case below, please.
In the case of the device states ready and DI="H" and DI/DO="High-Z" or DI/DO="H", if controller output "H" to SK, the device may be recognized as start bit unintentional and occur malfunction.
Keep SK="L" during DO output READY, please.
OR
Bring CS "L" within 4 clock cycle after READY/BUSY signal turn to "H", please. (See Fig.7-4)



Because of DI="H",
SK input need to be "L"
when CS is brought high

Fig.7-4 RECOMMENDED TIMING
DURING DO OUTPUTS READY

○VALUE OF RESISTER

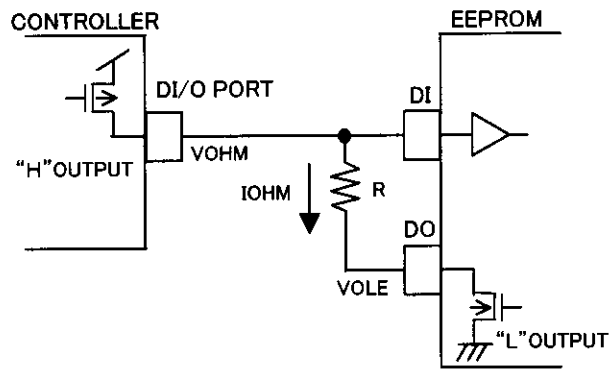
"R" is current limit resister during conflict on the bus. The current overload may cause noises on the power line and instantaneous power down.

The following conditions must be met, where "I" is the maximum permissible current. The maximum permissible current depends on Vcc line impedance and so on.

Value of "R" need to be decided to meet VIH/VIL specification of EEPROM even if there are some leakage current. The insert on "R" does not make any problem for function.

(1)When the device receives DI="1"(A0="1") and outputs DO="0"(dummy="0")
(CONTROLLER"H"OUTPUT, EEPROM:DO="L"OUTPUT,DI="H"INPUT)

- IOHM needs to be less than 10mA for EEPROM.
- VOHM needs to be less than VIHE as following.



Condition

$$VOHM \leqq VIHE$$

$$VOHM \leqq IOHM \times R + VOLE$$

When VOLE=0V,

$$VOHM \leqq IOHM \times R$$

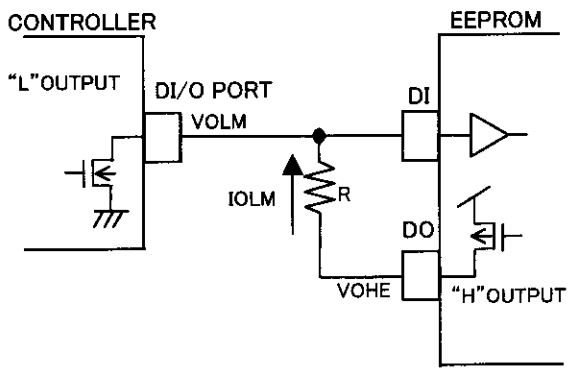
$$\therefore \quad R \geqq \frac{VOHM}{IOHM} \cdots ⑦$$

Fig.7-5 DI/O PORT TO CONNECT DI AND DO
(CONTROLLER "H" OUTPUT,
EEPROM "L" OUTPUT)

- VIHE : VIH specification of EEPROM
- VOLE : VOL specification of EEPROM
- VOHM : VOH specification of CONTROLLER
- IOHM : IOH specification of CONTROLLER

(2)When DO state is "H"(READY)
(CONTROLLER"L"OUTPUT, EEPROM:DO="H"OUTPUT,DI="L"INPUT)

- VOLM needs to be less than VILE as following.



Condition

$$VOLM \geqq VILE$$

$$VOLM \geqq VOHE - IOLM \times R$$

When VOHE=Vcc,

$$VOLM \geqq Vcc - IOLM \times R$$

$$\therefore \quad R \geqq \frac{Vcc - VOLM}{IOLM} \cdots ⑧$$

Fig.7-6 DI/O PORT TO CONNECT DI AND DO
(CONTROLLER "L" OUTPUT,
EEPROM "H" OUTPUT)

- VILE : VIL specification of EEPROM
- VOHE : VOH specification of EEPROM
- VOLM : VOL specification of CONTROLLER
- IOLM : IOL specification of CONTROLLER

Example) When Vcc=5V,VOHM=5V,IOHM=0.4mA,VOLM=5V,IOLM=0.4mA,

According to ⑦,

$$R \geqq \frac{VOHM}{IOHM}$$

$$R \geqq \frac{5}{0.4 \times 10^{-3}}$$

$$\therefore \quad R \geqq 12.5[k\Omega] \quad \cdots ⑨$$

According to ⑧,

$$R \geqq \frac{Vcc-VOLM}{IOLM}$$

$$R \geqq \frac{5-0.4}{2.1 \times 10^{-3}}$$

$$\therefore \quad R \geqq 2.2[k\Omega] \quad \cdots ⑩$$

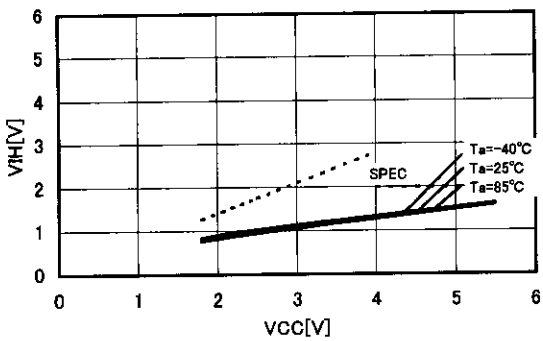
According to ⑨,⑩

$$\therefore \quad R \geqq 12.5[k\Omega]$$

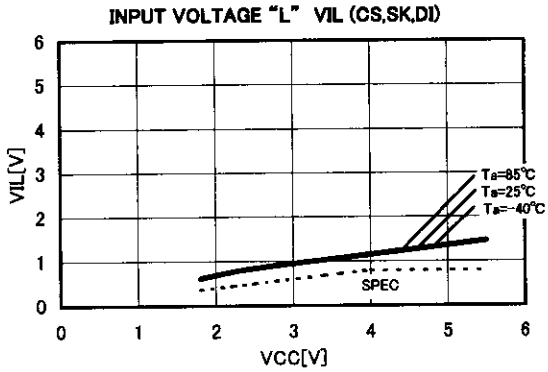
8) SPECIAL CHARACTERISTICS

The following characteristics data are typical value.

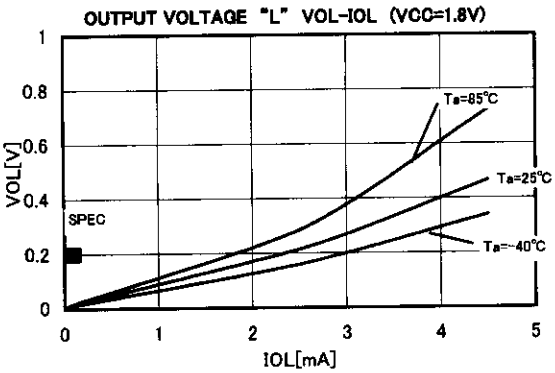
INPUT VOLTAGE "H" VIH (CS,SK,DI)



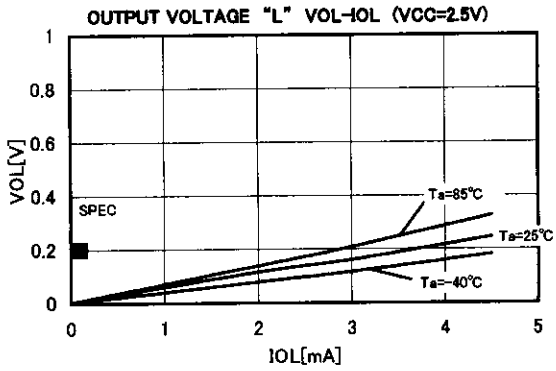
INPUT VOLTAGE "L" VIL (CS,SK,DI)



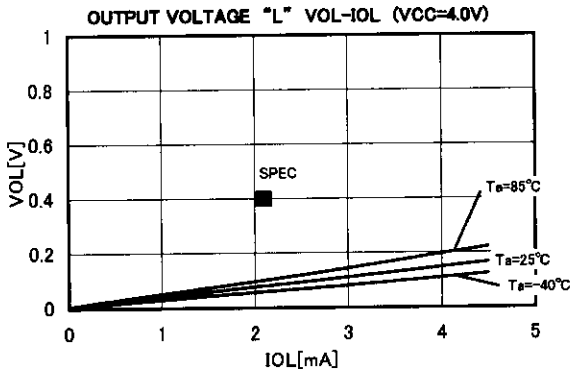
OUTPUT VOLTAGE "L" VOL-IOL (VCC=1.8V)



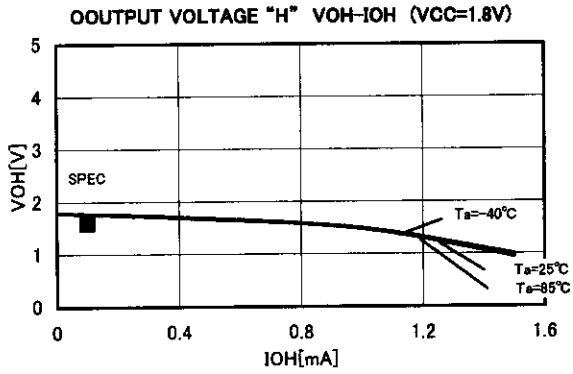
OUTPUT VOLTAGE "L" VOL-IOL (VCC=2.5V)



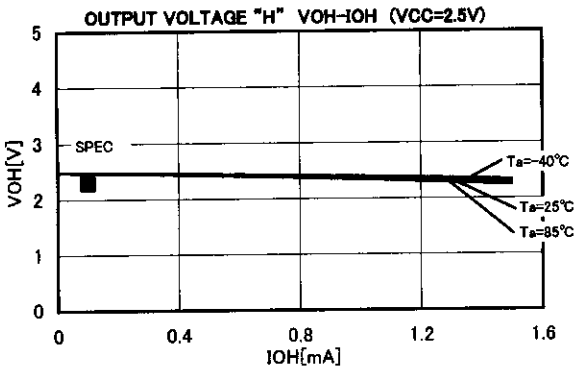
OUTPUT VOLTAGE "L" VOL-IOL (VCC=4.0V)



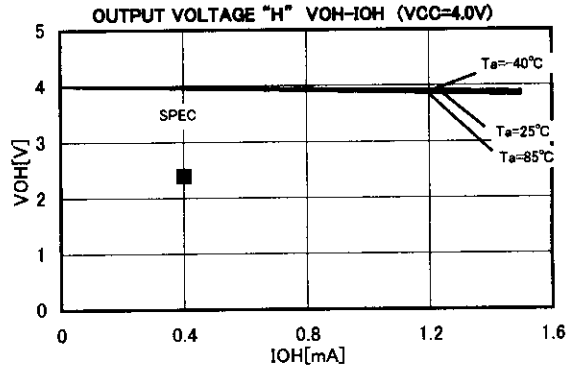
OOUTPUT VOLTAGE "H" VOH-IOH (VCC=1.8V)



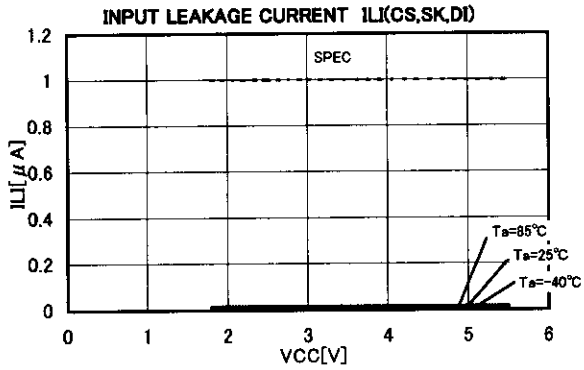
OUTPUT VOLTAGE "H" VOH-IOH (VCC=2.5V)



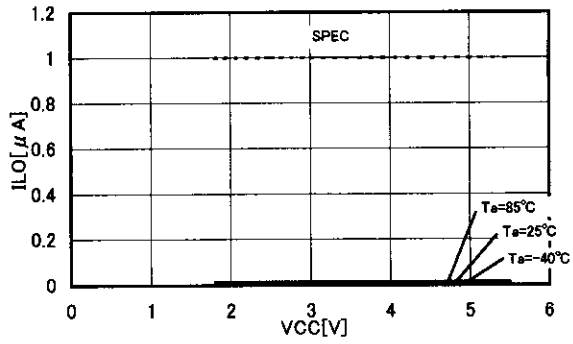
OUTPUT VOLTAGE "H" VOH-IOH (VCC=4.0V)



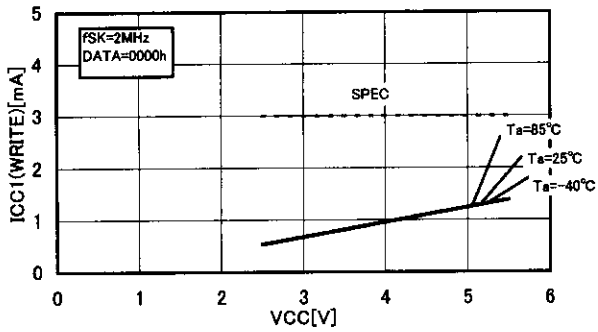
INPUT LEAKAGE CURRENT ILI(CS,SK,DI)



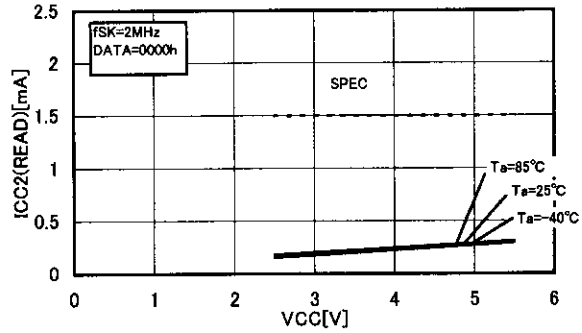
OUPUT LEAKAGE CURRENT ILO(DO)



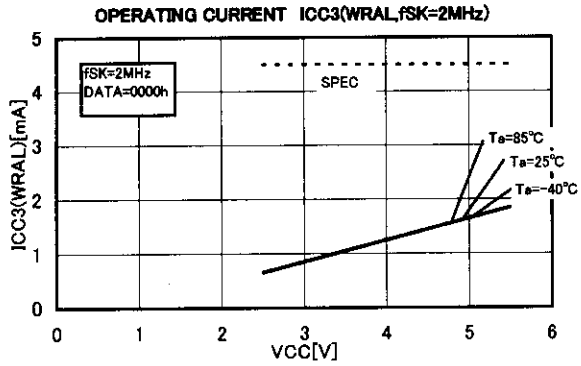
OPERATING CURRENT ICC1(WRITE,fSK=2MHz)



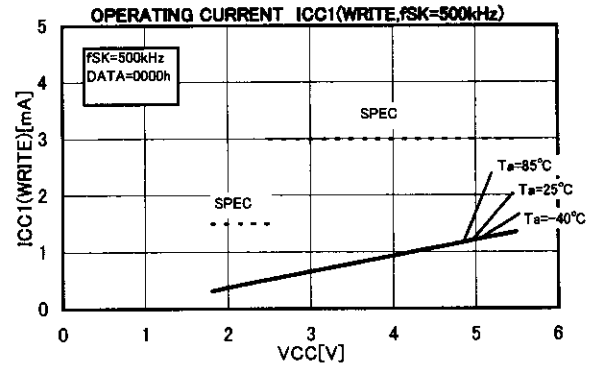
OPERATING CURRENT ICC2(READ,fSK=2MHz)



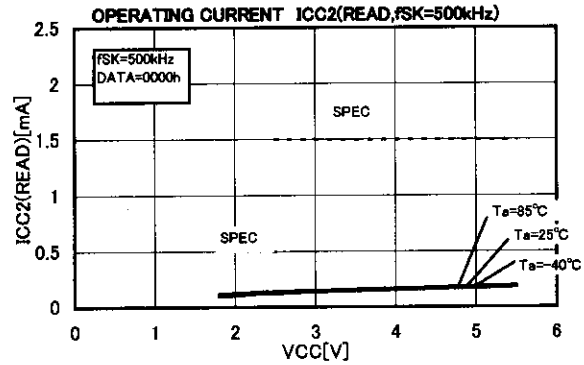
OPERATING CURRENT ICC3(WRAL,fSK=2MHz)



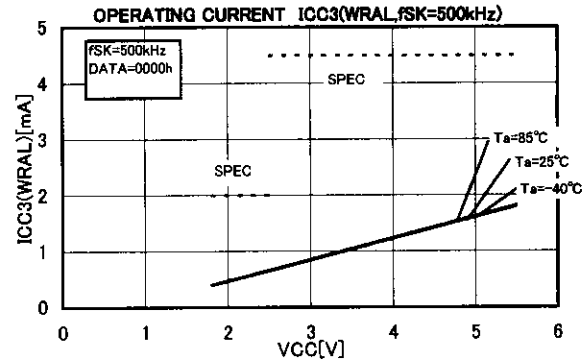
OPERATING CURRENT ICC1(WRITE,fSK=500kHz)

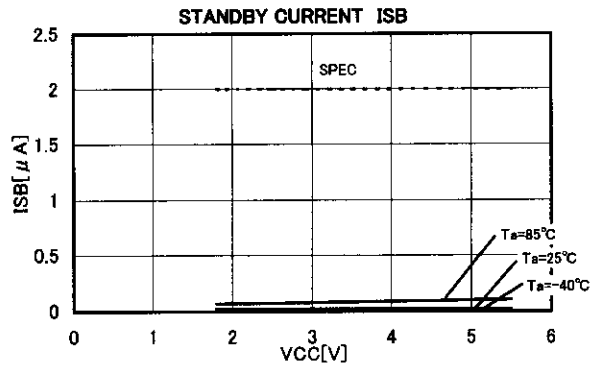


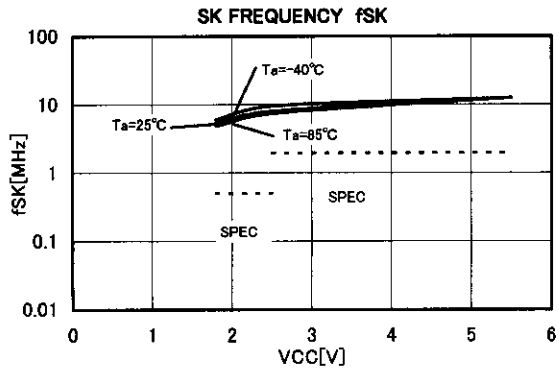
OPERATING CURRENT ICC2(READ,fSK=500kHz)

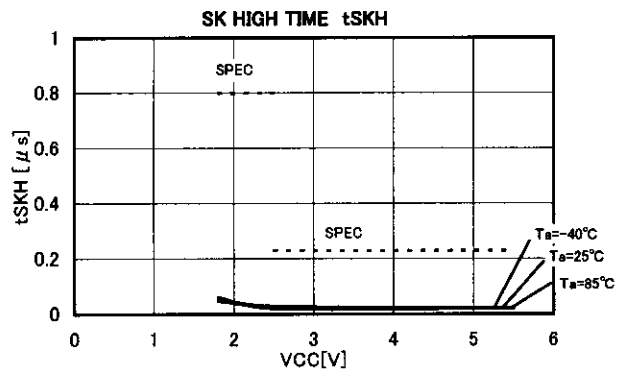


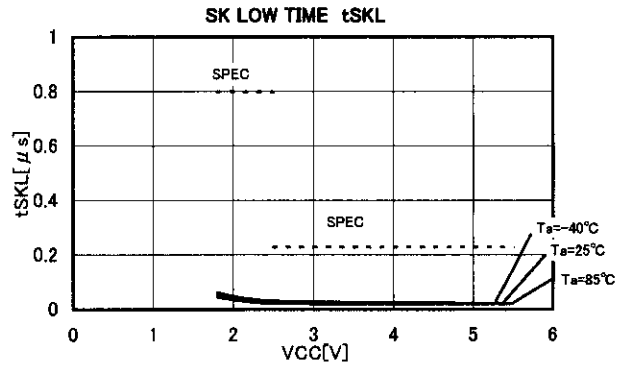
OPERATING CURRENT ICC3(WRAL,fSK=500kHz)

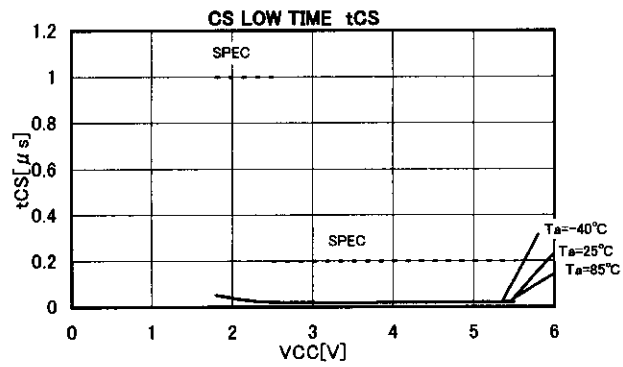


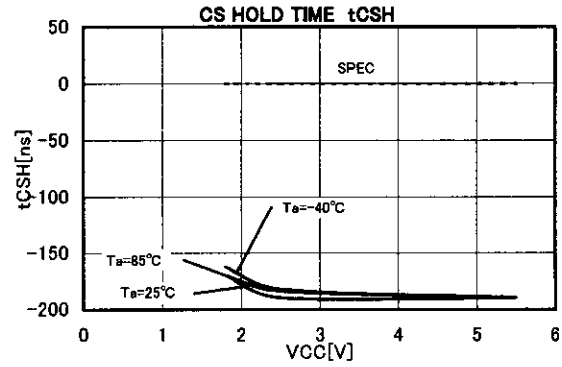

STANDBY CURRENT ISB
SPEC
Ta=85℃
Ta=25℃
Ta=-40℃
ISB[μA]
VCC[V]


SK FREQUENCY fSK
Ta=-40℃
Ta=25℃
Ta=85℃
SPEC
SPEC
fSK[MHz]
VCC[V]

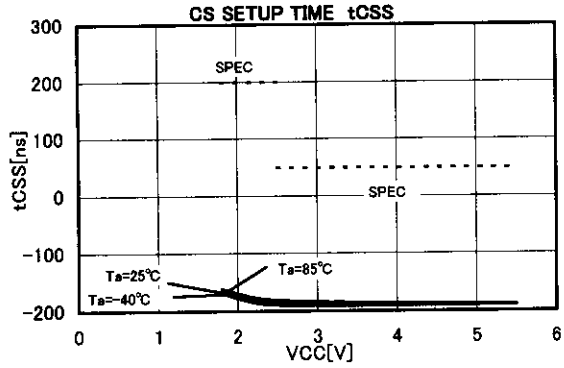

SK HIGH TIME tSKH
SPEC
SPEC
Ta=-40℃
Ta=25℃
Ta=85℃
tSKH[μs]
VCC[V]


SK LOW TIME tSKL
SPEC
SPEC
Ta=-40℃
Ta=25℃
Ta=85℃
tSKL[μs]
VCC[V]

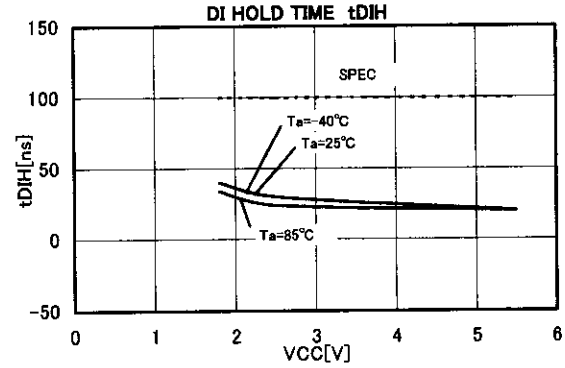

CS LOW TIME tCS
SPEC
SPEC
Ta=-40℃
Ta=25℃
Ta=85℃
tCS[μs]
VCC[V]


CS HOLD TIME tCSH
SPEC
Ta=-40℃
Ta=85℃
Ta=25℃
tCSH[ns]
VCC[V]

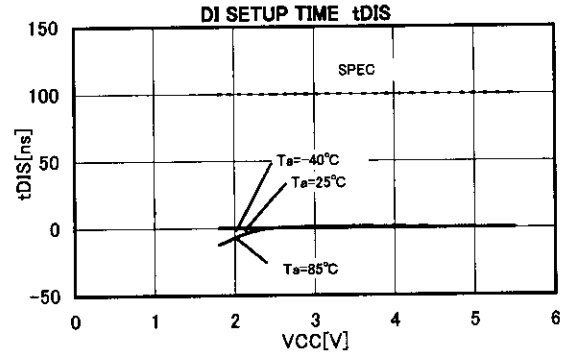
CS SETUP TIME tCSS



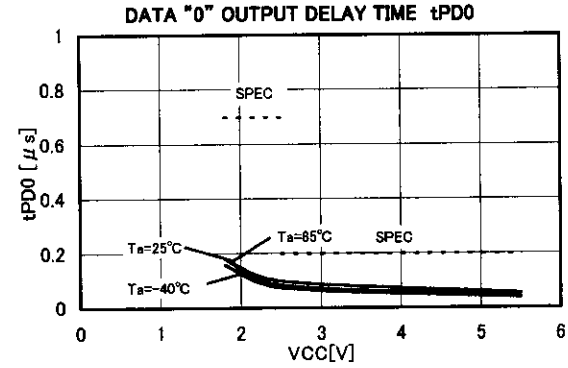
DI HOLD TIME tDIH



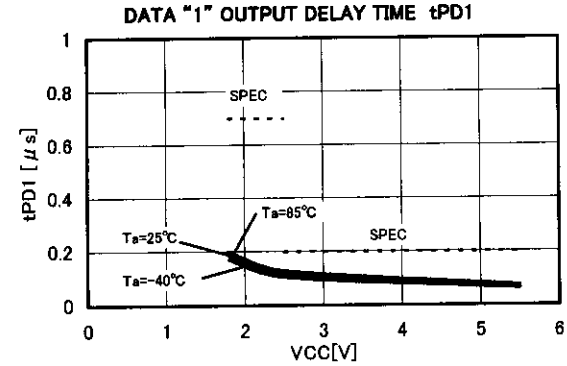
DI SETUP TIME tDIS



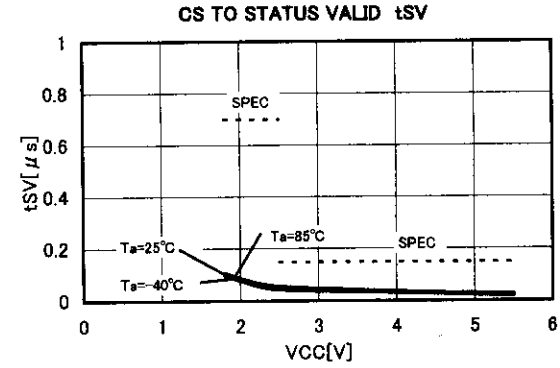
DATA "0" OUTPUT DELAY TIME tPD0



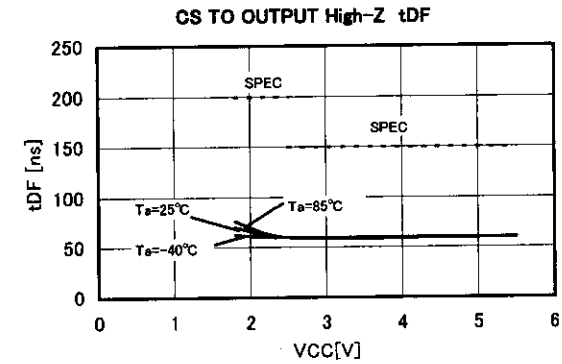
DATA "1" OUTPUT DELAY TIME tPD1



CS TO STATUS VALID tSV



CS TO OUTPUT High-Z tDF



WRITE CYCLE TIME tE/W