CMOS VOLTAGE DETECTOR IC with Delay Time Circuit

BD52XXG/FVE
BD53XXG/FVE

ROHM's BD52XXG/FVE and BD53XXG/FVE are series of high-accuracy, low-power VOLTAGE DETECTOR ICs with a CMOS process. These series can set delay time by external capacitor. For flexible choice according to the application, BD52XXG/FVE series with N channel open drain output and BD53XXG/FVE series with CMOS output are available in 38 voltage types which detection voltage is from 2.3V to 6.0V in steps of 0.1V in different packages, totaling 152 models.

● Applications

Every kind of appliances with microcontroller and logic circuit

● Features

1) Detection voltage: 0.1V step line-up 2.3 to 6.0V (Typ.)
2) High-accuracy detection voltage: ±1.5% guranteed (Ability ±1%)
3) Ultra low current consumption: 0.85μA typ. (Output is High.)
4) Delay time can be set by external capacitor.
5) Nch open drain output (BD52XXG/FVE series), CMOS output (BD53XXG/FVE series)
6) Small package of VSOF5(EMP5)(BD52XXFVE/BD53XXFVE), and SSOP5(SMP5C2)(BD52XXG/BD53XXG)

● Selection guide

For BD5XXXX series, detection voltage, output circuit types (Refer to the block diagram at P3),and package (Refer to the block diagram at P14) can be selected for your own application.Part number of devices for each specification is shown below.

Part No. : B D 5 X X X X

① ② ③

Part No.	Specification	Contents
①	Output circuit types	2 : Open drain output 3 : CMOS output
②	Detection voltage	Ex. : V_{DET} : described in each 0.1V step for 2.3V to 6.0V range (29 means 2.9V)
③	Package	G : SSOP5 (SMP5C2) FVE : VSOF5 (EMP5)

● Line-up

Detection voltage V_{DET}	Nch Open drain output (BD52XXG/FVE)	CMOS output (BD53XXG/FVE)	Detection voltage V_{DET} (V) Ta=25℃			Hysteresis voltage (V,Typ.)	Package
			Min.	Typ.	Max.		
6.0V	BD5260G/FVE	BD5360G/FVE	5.910	6.000	6.090	V_{DET}X 0.05	SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.9V	BD5259G/FVE	BD5359G/FVE	5.812	5.900	5.989		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.8V	BD5258G/FVE	BD5358G/FVE	5.713	5.800	5.887		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.7V	BD5257G/FVE	BD5357G/FVE	5.615	5.700	5.786		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.6V	BD5256G/FVE	BD5356G/FVE	5.516	5.600	5.684		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.5V	BD5255G/FVE	BD5355G/FVE	5.418	5.500	5.583		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.4V	BD5254G/FVE	BD5354G/FVE	5.319	5.400	5.481		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.3V	BD5253G/FVE	BD5353G/FVE	5.221	5.300	5.380		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.2V	BD5252G/FVE	BD5352G/FVE	5.122	5.200	5.278		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.1V	BD5251G/FVE	BD5351G/FVE	5.024	5.100	5.177		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.0V	BD5250G/FVE	BD5350G/FVE	4.925	5.000	5.075		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.9V	BD5249G/FVE	BD5349G/FVE	4.827	4.900	4.974		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.8V	BD5248G/FVE	BD5348G/FVE	4.728	4.800	4.872		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.7V	BD5247G/FVE	BD5347G/FVE	4.630	4.700	4.771		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.6V	BD5246G/FVE	BD5346G/FVE	4.531	4.600	4.669		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.5V	BD5245G/FVE	BD5345G/FVE	4.433	4.500	4.568		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.4V	BD5244G/FVE	BD5344G/FVE	4.334	4.400	4.466		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.3V	BD5243G/FVE	BD5343G/FVE	4.236	4.300	4.365		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.2V	BD5242G/FVE	BD5342G/FVE	4.137	4.200	4.263		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.1V	BD5241G/FVE	BD5341G/FVE	4.039	4.100	4.162		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.0V	BD5240G/FVE	BD5340G/FVE	3.940	4.000	4.060		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.9V	BD5239G/FVE	BD5339G/FVE	3.842	3.900	3.959		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.8V	BD5238G/FVE	BD5338G/FVE	3.743	3.800	3.857		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.7V	BD5237G/FVE	BD5337G/FVE	3.645	3.700	3.756		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.6V	BD5236G/FVE	BD5336G/FVE	3.546	3.600	3.654		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.5V	BD5235G/FVE	BD5335G/FVE	3.448	3.500	3.553		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.4V	BD5234G/FVE	BD5334G/FVE	3.349	3.400	3.451		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.3V	BD5233G/FVE	BD5333G/FVE	3.251	3.300	3.350		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.2V	BD5232G/FVE	BD5332G/FVE	3.152	3.200	3.248		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.1V	BD5231G/FVE	BD5331G/FVE	3.054	3.100	3.147		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.0V	BD5230G/FVE	BD5330G/FVE	2.955	3.000	3.045		SSOP5 (SMP5C2) / VSOF5 (EMP5)
2.9V	BD5229G/FVE	BD5329G/FVE	2.857	2.900	2.944		SSOP5 (SMP5C2) / VSOF5 (EMP5)
2.8V	BD5228G/FVE	BD5328G/FVE	2.758	2.800	2.842		SSOP5 (SMP5C2) / VSOF5 (EMP5)
2.7V	BD5227G/FVE	BD5327G/FVE	2.660	2.700	2.741		SSOP5 (SMP5C2) / VSOF5 (EMP5)
2.6V	BD5226G/FVE	BD5326G/FVE	2.561	2.600	2.639		SSOP5 (SMP5C2) / VSOF5 (EMP5)
2.5V	BD5225G/FVE	BD5325G/FVE	2.463	2.500	2.538		SSOP5 (SMP5C2) / VSOF5 (EMP5)
2.4V	BD5224G/FVE	BD5324G/FVE	2.364	2.400	2.436		SSOP5 (SMP5C2) / VSOF5 (EMP5)
2.3V	BD5223G/FVE	BD5323G/FVE	2.266	2.300	2.335		SSOP5 (SMP5C2) / VSOF5 (EMP5)

● Pin layout

Pin layout of VSOF5(EMP5) and SSOP5(SMP5C2) is different as shown below. (Fig.1, Fig.2)
When used as replacement, please consider the difference. (The detail of packages is shown at P14.)

BD52XXFVE/BD53XXFVE

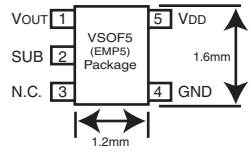


Fig.1

BD52XXG/BD53XXG

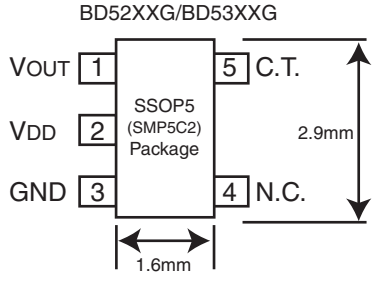


Fig.2

(Note) Connect SUB pin with GND pin.

● Block diagram

Two output types can be used. One is BD52XXG/FVE (Left) of open drain output type, and the other is BD53XXG/FVE (Right) of CMOS output type.

BD52XXG/FVE : Open drain output

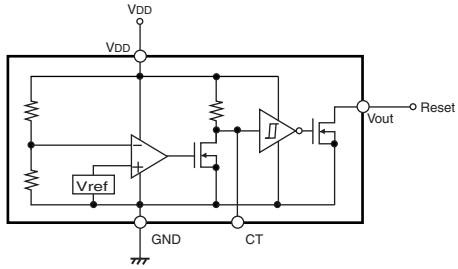


Fig.3

BD53XXG/FVE : CMOS output

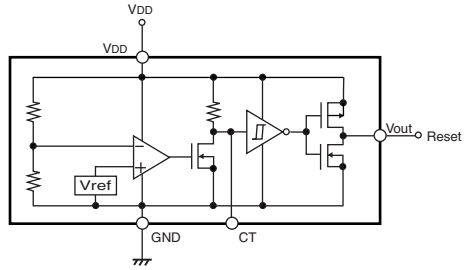


Fig.4

● Absolute maximum rating (Ta=25°C)

To prevent the functional deterioration or thermal damage of semiconductor devices and ensure their service life and reliability, they must be designed and reviewed in such a way that the absolute maximum rating can not be exceeded in any cases or even at any moment.

Parameter		Symbol	Limits	Unit
Power supply voltage		V_{DD} – GND	– 0.3 to + 10	V
Output voltage	Nch Open drain output	V_{OUT}	GND – 0.3 to + 10	V
	CMOS output		GND – 0.3 to V_{DD} + 0.3	
CT pin voltage		V_{CT}	GND – 0.3 to V_{DD} + 0.3	V
Power dissipation (SSOP5(SMP5C2)) *1 *3		Pd	540	mW
Power dissipation (VSOF5(EMP5)) *2 *3		Pd	210	mW
Operating temperature		T_{opr}	– 40 to + 85	°C
Storage temperature		T_{stg}	– 55 to + 125	°C

*1 Derating : 5.4mW/°C for operation above Ta=25°C
*2 Derating : 2.1mW/°C for operation above Ta=25°C
*3 When ROHM's standard board(70mmX70mmX1.6mm, glass epoxy board) is mounted.

- Power supply voltage

  This voltage is the applied voltage between V_{DD} and GND. The applied voltage should not exceed the indicated value.

- Output voltage

  V_{OUT} pin voltage should not exceed the indicated value. For Nch open drain output type, V_{DD} applied voltage and V_{OUT} pin H output voltage can be used independently. Both of them should not exceed the each indicated value.

- Operating temperature range

  The circuit function is guaranteed within the temperature range. However, the operating characteristics are different from that of Ta=25°C. If they are any questions about the extent of guarantee of circuit functions in this operating temperature range, please ask for more technical information.

- Storage temperature range

  This IC can be stored up to this temperature range without deterioration of characteristics. However, an abrupt thermal shock of extreme temperature fluctuations may cause the deterioration of characteristics.

● Power dissipation

Power consumption of the IC

Circuit current at ON/OFF is very small. Power consumption in output depends on each load connected with VOUT pin. Please note that total power consumption must be within a power dissipation range in the secure area of the entire operating temperature. Power dissipation of these packages; SSOP5 (SMP5C2) package (BD52XXG/ BD53XXG) Fig.5, and VSOF5 (EMP5) package (BD52XXFVE/BD53XXFVE) Fig.6 is shown below.

SSOP5 (SMP5C2) package

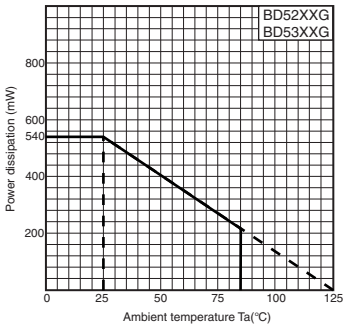


Fig.5 Thermal derating curve

VSOF5 (EMP5) package

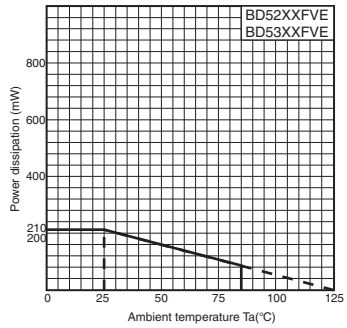


Fig.6 Thermal derating curve

When it is used in the ambient temperature of (Ta)=25℃ and more, make reference to each thermal derating characteristics of used package. Both Fig.5 and Fig.6 show these characteristic when ROHM's standard board (70mmX70mmX1.6mm, glass epoxy board) is mounted.

● Electrical characteristics (Unless otherwise noted; Ta=-25℃ to 85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions		Reference Data
Detection voltage temperature coefficient	VDET/ΔT	—	±100	±360	ppm/℃			Fig.30
Hysteresis voltage	ΔVDET	VDETX0.03	VDETX0.05	VDETX0.08	V	RL=470kΩ, VDD=L→H→L		Fig.28
Circuit current when ON	IDD1	—	0.80	2.40	μA	VDD=VDET–0.2V	VDET=2.3 to 3.1V	Fig.25
		—	0.85	2.55			VDET=3.2 to 4.2V	
		—	0.90	2.70			VDET=4.3 to 5.2V	
		—	0.95	2.85			VDET=5.3 to 6.0V	
Circuit current when OFF	IDD2	—	0.75	2.25	μA	VDD=VDET+2.0V	VDET=2.3 to 3.1V	
		—	0.80	2.40			VDET=3.2 to 4.2V	
		—	0.85	2.55			VDET=4.3 to 5.2V	
		—	0.90	2.70			VDET=5.3 to 6.0V	
Min. operating voltage	VOPL	0.95	—	—	V	RL=470k , VOL 0.4V		Fig.34
"L" output current	IOL1	0.4	1.2	—	mA	VDS=0.5V, VDD=1.2V	VDET=2.3 to 6.0V	Fig.26
	IOL2	2.0	5.0	—		VDS=0.5V, VDD=2.4V	VDET=2.7 to 6.0V	
"H" output current (Only BD53XXG/FVE series)	IOH	0.7	1.4	—	mA	VDS=0.5V, VDD=4.8V	VDET=2.3 to 4.2V	Fig.27
		0.9	1.8	—		VDS=0.5V, VDD=6.0V	VDET=4.3 to 5.2V	
		1.1	2.2	—		VDS=0.5V, VDD=8.0V	VDET=5.3 to 6.0V	
CT pin Threshold voltage	VCTH	VDDX0.3	VDDX0.4	VDDX0.6	V	VDD=VDETX1.1 RL=470k	VDET=2.3 to 2.6V	Fig.35
		VDDX0.3	VDDX0.45	VDDX0.6			VDET=2.7 to 4.2V	
		VDDX0.35	VDDX0.5	VDDX0.6			VDET=4.3 to 5.2V	
		VDDX0.4	VDDX0.5	VDDX0.6			VDET=5.3~6.0V	
CT pin	RCT	5.5	9	12.5	MΩ	VDD=VDETX1.1, VCT=0.5V *1		Fig.36
CT pin "L" current	ICT1	15	40	—	μA	VCT=0.1V,VDD=0.95V *1		Fig.37
	ICT2	150	240	—		VCT=0.5V,VDD=1.5V		
Output leak current	Ileak	—	—	0.1	μA	VDD=VDS=10V *1		Fig.32

*1 Operation is guaranteed for Ta=25℃.
Note) RL is not necessary for CMOS output type.
Note) Minimum operating voltage
VOUT output becomes inconsistent if the VDD is equal to or lower than the operating limit voltage. It goes open, H, or L.
Note) Hysteresis voltage=(Reset release voltage)-(Reset detection voltage) [V]

● Term explanation

①Detection voltage (VDET) : VDD voltage when the output (Vout) goes from “H” to “L” .
②Release voltage (VDET+ΔVDET) : VDD voltage when output (Vout) goes from “L” to “H” .
③Hysteresis voltage (ΔVDET) : The difference between detection voltage and release voltage. Malfunction due to noise in VDD (within hysteresis voltage) could be avoided by hysteresis voltage.

● Operating explanation

Ex.) For both open drain type (Fig.7) and CMOS output type (Fig.8), detection voltage and release voltage are threshold voltage. When voltage applied to VDD pin reaches each threshold voltage, VOUT pin voltage goes "H"→"L" or "L"→"H'. BD52XXG/FVE and BD53XXG/FVE incorporate delay time circuit that can set delay time by the external capacitor when output goes"L"→"H". BD52XXG/FVE series are open drain types and pull-up resistor must be connected to VDD, or other power supply. (In this case, output (VOUT) H voltage is VDD, or other power supply voltage.)

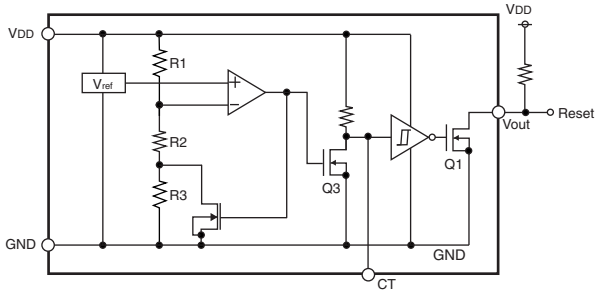


Fig.7 (BD52XX type Internal block diagram)

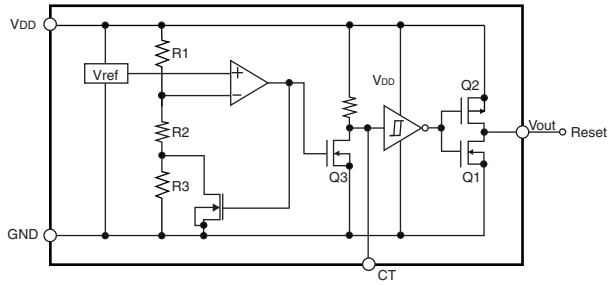


Fig.8 (BD53XX Internal block diagram)

• SWEEP DOWN for VDD

•When VDD is equal to or more than the release voltage (VDET+ΔVDET), CT pin voltage becomes VDD (External capacitor is in charging mode.) and output VOUT is in "H" mode. (Nch output transistor Q1 is OFF, Pch output transistor Q2 is ON.) When VDD is gradually decreased, Q3 connected to CT pin in the detection voltage (VDET) switches OFF to ON, external capacitor is discharged, and CT pin voltage becomes decreased. When the CT pin voltage is lower than the threshold voltage of next inverter, output (VOUT) turns "L". (Nch output transistor Q1 is ON, Pch output transistor Q2 is OFF.)

• SWEEP UP for VDD

• When VDD is equal to or lower than the detection voltage (VDET), CT pin voltage is L voltage (External capacitor is in discharging mode and Q3 is ON), output VOUT is in "L" mode. When VDD is gradually increased, Q3 is OFF in the release voltage (VDET+ΔVDET) and CT pin external capacitor becomes to be charged through resistor R1 in the IC. When the CT pin voltage is more than the threshold voltage of next inverter, output (VOUT) goes from "L" to "H". (Nch output transistor Q1 is OFF, Pch output transistor Q2 is ON.) Delay time is the time when output VOUT goes from "L" to "H" after the VDD is more than the release voltage. (VDET+ΔVDET) Delay time can be set freely by the CT pin external capacitor. (Usage is shown at P10)

•Some hysteresis is given such a way that the release voltage is the detection voltageX(1.05 Typ.).

• The output becomes inconsistent if the VDD is equal to or lower than the operating limit voltage.

● Timing waveform

Ex.) The relation between input voltage VDD and output voltage VOUT when VDD is increased and decreased is shown below. (Circuit is shown in Fig7, Fig.8)

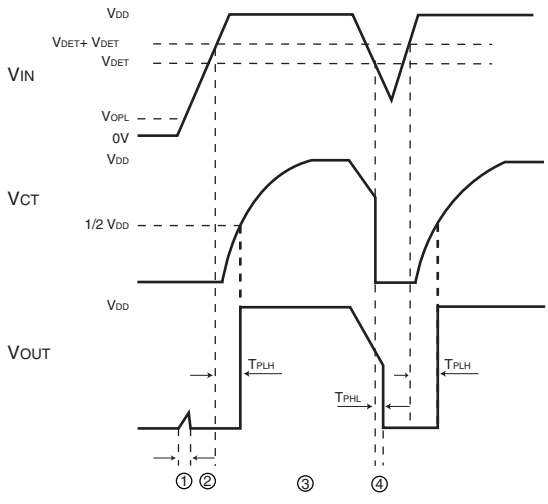


Fig.9

① If the VDD is equal to or lower than the operating limit voltage (VOPL) at power-up, the output is inconsistent.

② When the VDD is equal to or more than the VOPL and the VDD is equal to or more than the reset release voltage (VDET+ΔVDET), CT pin voltage (VCT) is "L" and output (VOUT) is also "L".

③ When the VDD is equal to or more than reset release voltage (VDET+ΔVDET), VOUT goes from "L" to "H" with a delay of TPLH set by the capacitor that is connected to CT pin.

④ If the VDD goes below the detection voltage (VDET) at power-down or instantaneous power failure, VOUT turns L with a delay of TPHL. See Fig.16 for the reference waveform. The potential difference between the detection voltage and the release voltage is called hysteresis (ΔVDET). The products are designed so as to prevent power supply fluctuation within this hysteresis from causing fluctuation in output in order to avoid malfunction due to noise.

● Application circuit

1) Application circuit as ordinal supply detection reset is shown below.

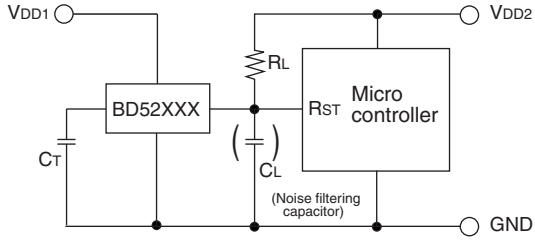


Fig.10 Open collector output type

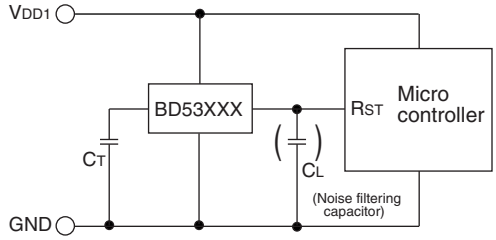


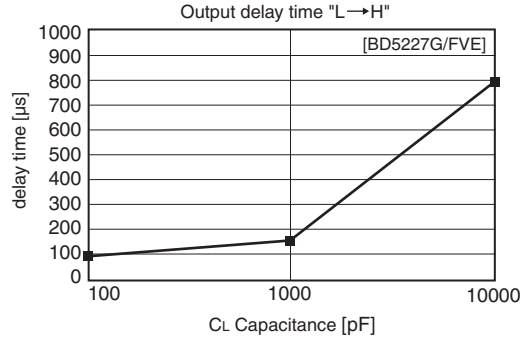
Fig.11 CMOS output type

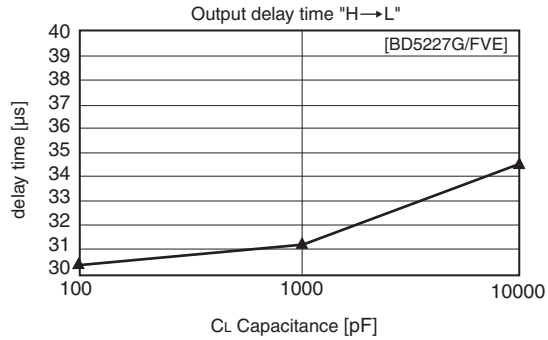
Output type of BD52XXG/FVE series (Open drain type) and BD53XXG/FVE series (CMOS type) is different. An example of usage is shown below.

① When the power supply of microcontroller (V_{DD2}) and power supply for the reset detection (V_{DD1}) is different. Provide RL for the output of a product with open drain output (BD52XXG/FVE series) on the V_{DD2} side, as shown in Fig.10.

② When the power supply of microcontroller and that of reset is same (V_{DD1}).
A product with CMOS output (BD53XXG/FVE series) can be used as shown in Fig.11. Or if RL is provided with open drain output (BD52XXG/FVE series) on the V_{DD1} side, it can be used.

When the capacitor C_L for noise filtering is connected to V_{OUT} pin (reset signal input pin of microcontroller), make a setting in consideration of the wave rounding of the rise and fall of V_{OUT} pin.





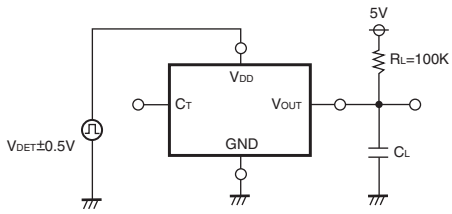


Fig.12

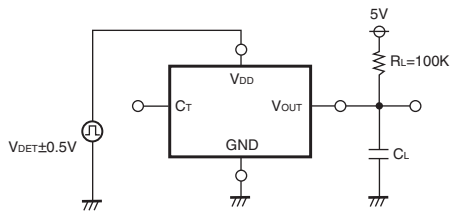


Fig.13

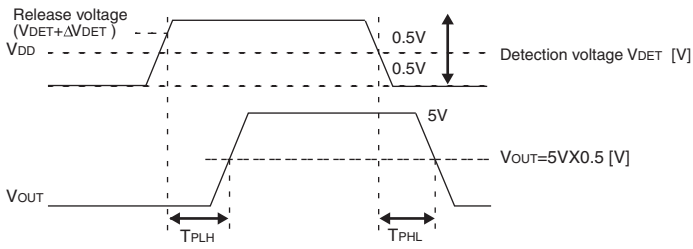


Fig.14 Delay time I/O condition

• Test data

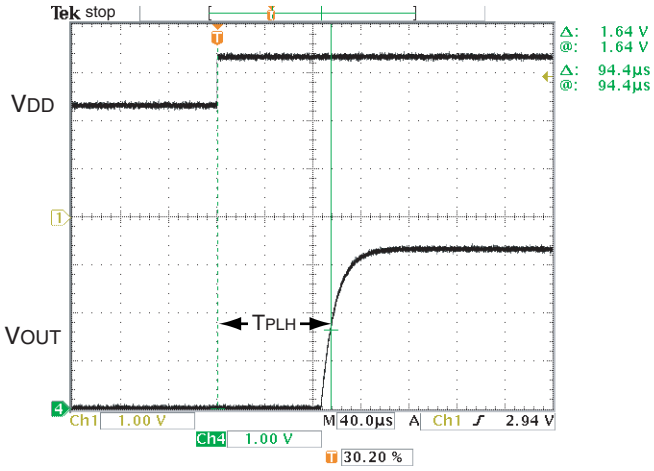


Fig.15
BD5227G TPLH output waveform

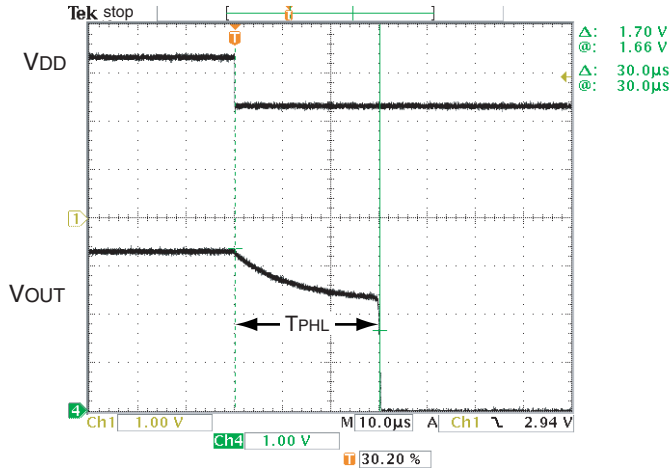


Fig.16
BD5227G TPHL output waveform

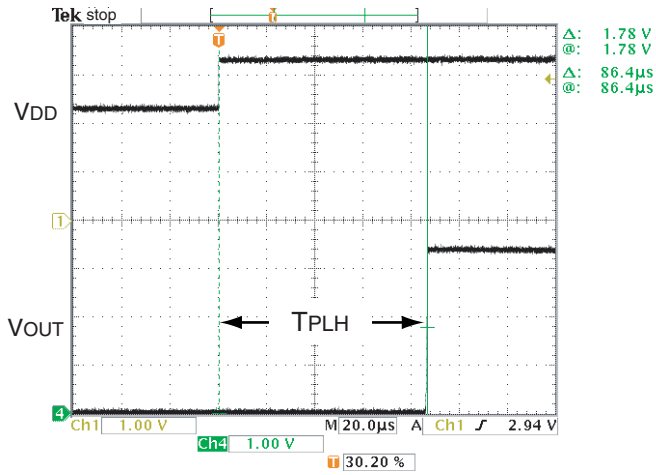


Fig.17
BD5327G TPLH output waveform

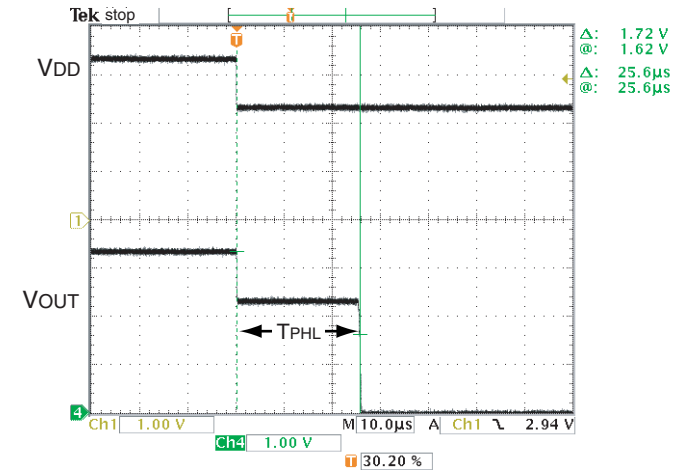
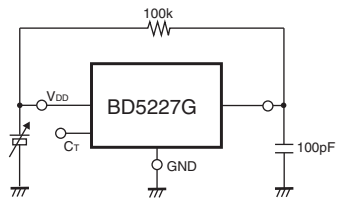
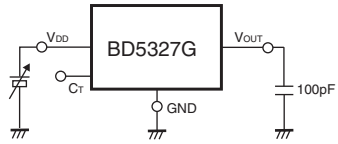


Fig.18
BD5327G TPHL output waveform

Reference data : BD5227G test data
RL=100kΩ
CL=100pF



Reference data : BD5327G test data
CL=100pF



2)Application circuit when microcontroller is reset with OR connection of the two types of the detection voltage is shown below.

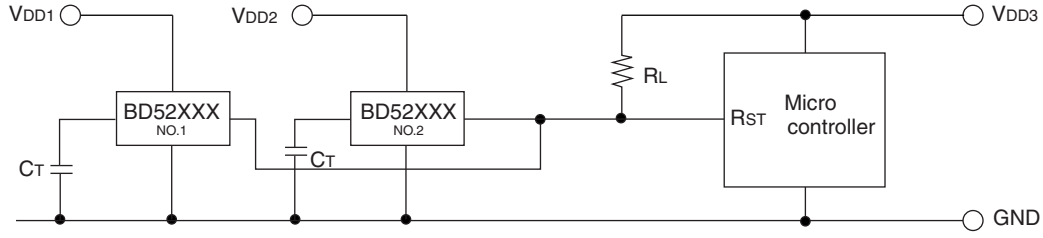
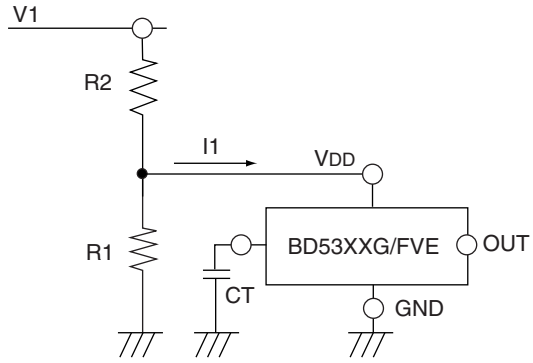


Fig.19

When there is more than one system power supply and it is necessary to individually monitor the power supply (V_{DD1}, V_{DD2}) to reset the microcontroller, open drain output type BD52XXG/FVE series can be connected to form an OR circuit as shown in Fig.19 for pulling up to an arbitrary voltage (V_{DD3}) to adjust the H voltage of the output to the microcontroller power supply (V_{DD3}).

For applications that voltage divided by resistance is inputted to input pin (V_{DD}) of the IC if BD53XXG/FVE with CMOS output is used, the feed through current is flowed instantly and it may cause malfunction (Oscillation at output etc.) when output goes "H" ↔ "L". (Feed through current is the current flowed from V_{DD} into GND instantly when output goes "H" ↔ "L".)



Voltage drop ([Feed through current I1] X [Input resistor R2]) is occurred by the feed through current when output goes "L" to "H", and input voltage is decreased. When input voltage is decreased and become to be lower than detection voltage, output goes "H" to "L". At this time, no feed through current flows for output L and no voltage drop occurs. And output goes "L" to "H" again, feed through current flows and voltage drop is occurred. This operation is repeated. This means oscillation.

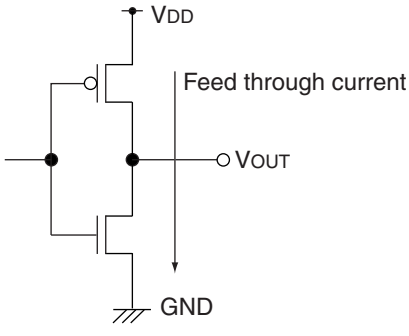


Fig.20
CMOS output circuit

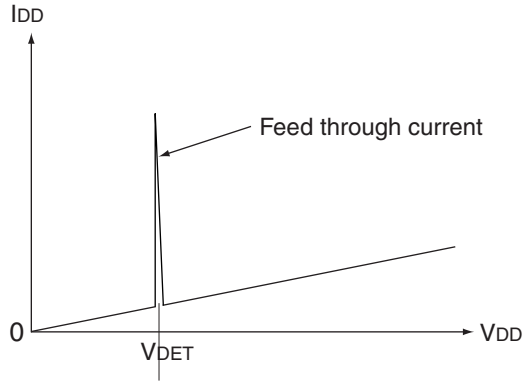


Fig.21
Current consumption Vs. power supply voltage

● Establishment of RESET transfer delay time

Delay time T_{PLH} at the rise of V_{DD} can be established by C_{CT} connected to C_T pin.

• Delay time at the rise of V_{DD} T_{PLH} : Time until when V_{OUT} is 1/2 of V_{DD} after the rise of V_{DD}, and beyond the release voltage ($V_{DET}+\Delta V_{DET}$).(See P7).

Expression (When the threshold voltage of next inverter connected to C_T pin is 1/2 of V_{DD}.)

$T_{PLH}=0.69XC_{CT}XR_{CT}$ (typ.)

C_{CT} : C_T pin external capacitor

R_{CT} : C_T pin internal impedance

ex) When C_T external capacitor is 0.047μF,

$T_{PLH}=0.69X0.047\mu FX9M\Omega$

≒292ms

Fig.22 shows the relation between capacity of external capacitor and delay time T_{PLH}.

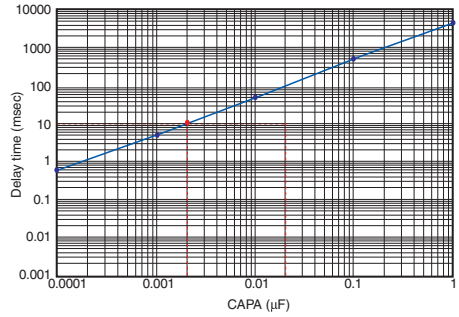


Fig.22
Delaly time(T_{PLH}) and external capacitance

• Delay time at the fall of V_{DD} T_{PHL} : Time until when V_{OUT} is 1/2 of V_{DD} after across the detection voltage (Vs).

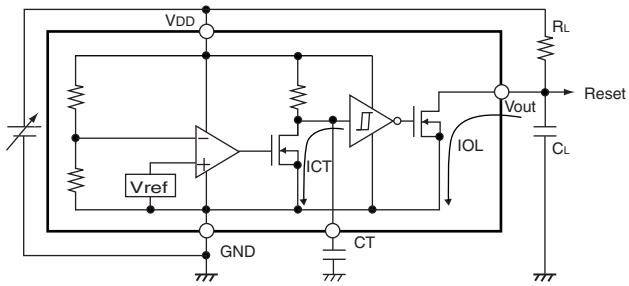


Fig.23

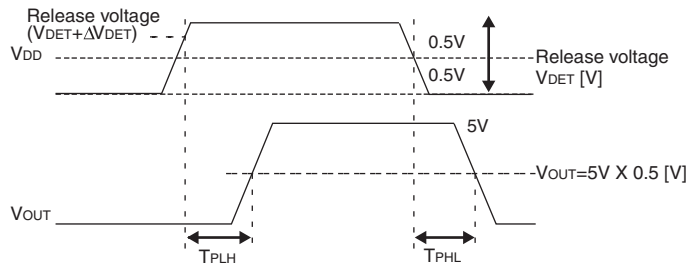


Fig.24 Delay time I/O condition

$T_{PHL}=T_A+T_B+T_C$

$T_A = \dfrac{C_L \times V_{DET}}{I_{OL}}$: Delay time by external C_L, R_L

C_L : Capacity of external capacitor beween V_{OUT} pin and GND

V_{DET} : Detection voltage

I_{OL} : "L" output current

(Make sure to test in actual because it depends on detection voltage.
Reference : V_{DET}=2.4V, V_{DD}=2.4V About 5mA : typ.)

$T_B = \dfrac{C_T \times V_{DET}}{I_{CT}}$: Delay time by external C of CT pin

(CT : External capacitor between CT pin and GND
V_{DET} : Detection voltage
I_{CT} : Output current of CT pin)

T_C = About 20.9μs(Typ.)IC internal transfer delay time

● Characteristic data (Reference data)

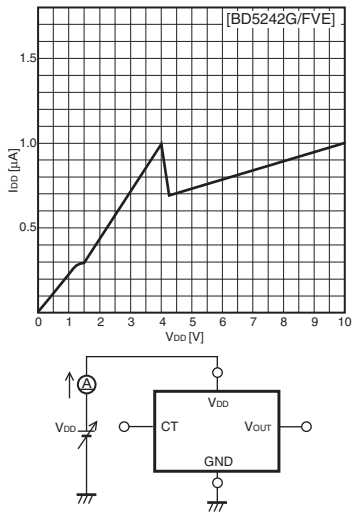


Fig.25
Circuit current

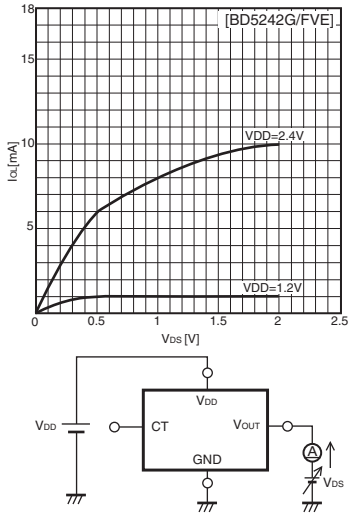


Fig.26
"L" output current

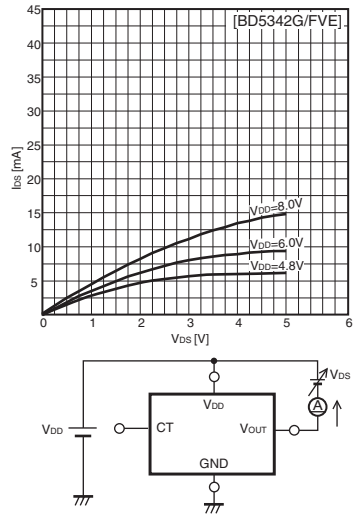


Fig.27
"H" output current

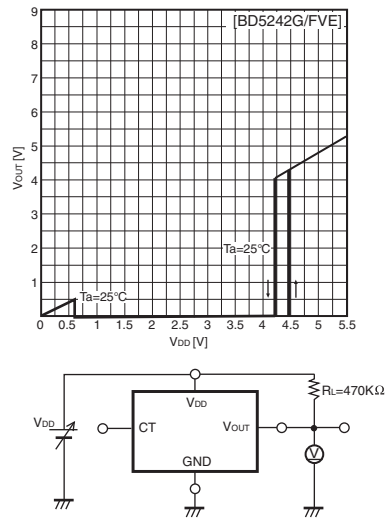


Fig.28
I/O characteristic

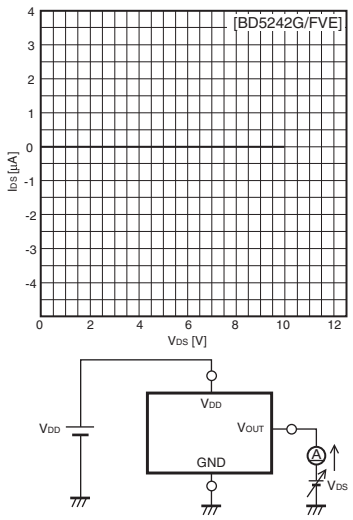


Fig.29
Output leak current

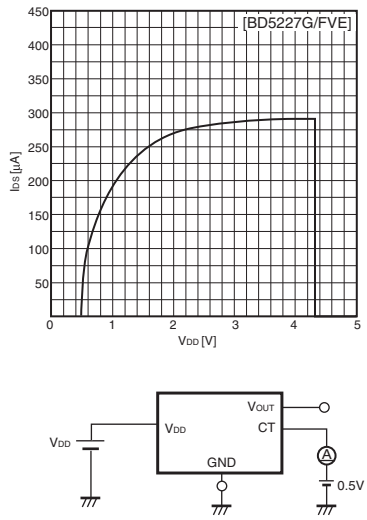


Fig.30
CT pin current

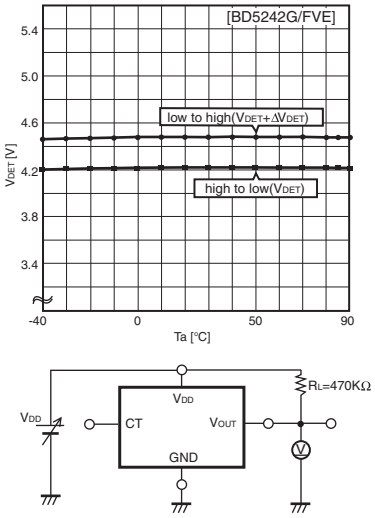


Fig.31 Detection voltage (V_{DET})
Release voltage ($V_{DET}+\Delta V_{DET}$)

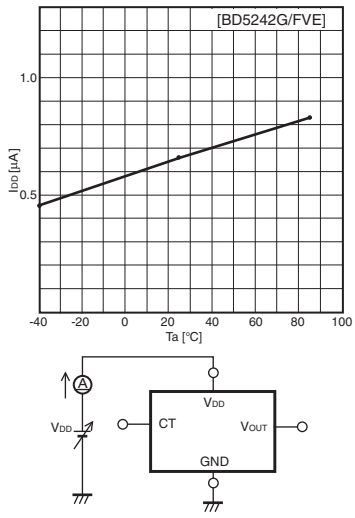


Fig.32 Circuit current when ON
(V_{DET}-0.2V)

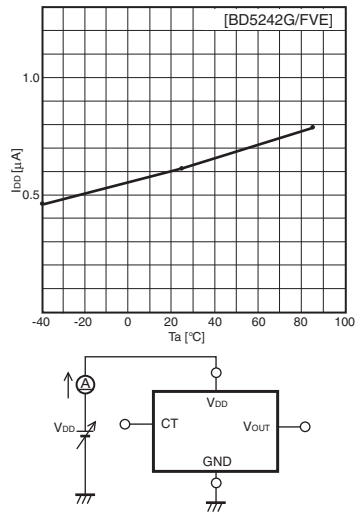


Fig.33 Circuit current when OFF
(V_{DET}+0.2V)

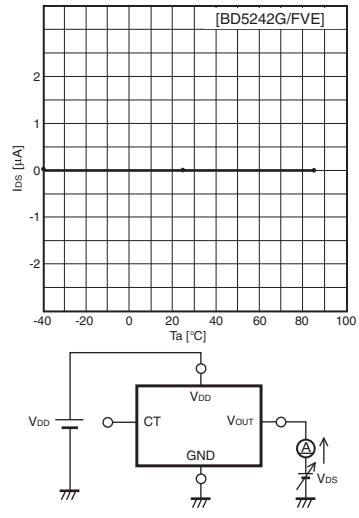


Fig.34 Output leak current

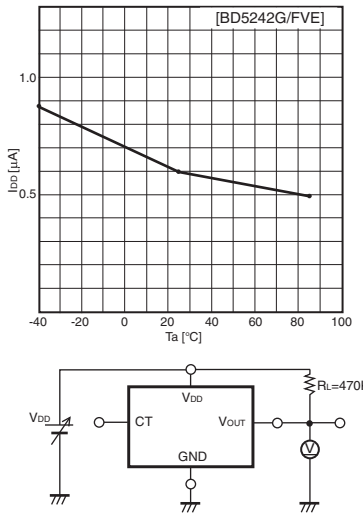


Fig.35 Operating limit voltage

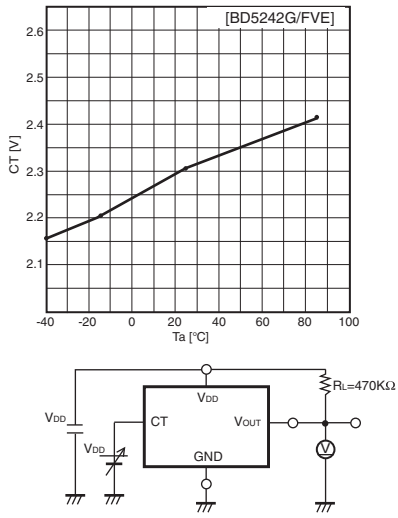


Fig.36 Threshold voltage

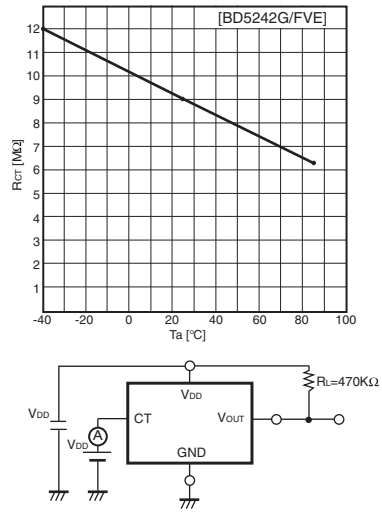


Fig.37 CT pin impedance

●Taping specification

1)Dimension of tape

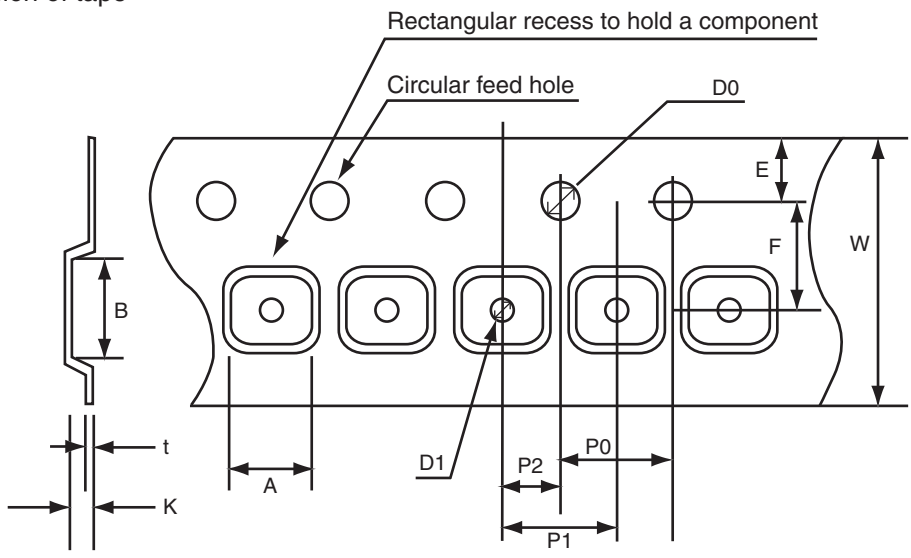


Fig.38

Package SSOP5 (SMP5C2) (mm)

Symbol	A	B	D0	D1	E	F	P0	P1	P2	t	K	W
Dimension	3.2±0.1	3.1±0.1	$1.5^{+0.1}_{-0}$	1.1±0.1	1.75±0.1	3.5±0.05	4.0±0.1	4.0±0.1	2.0±0.05	0.3±0.05	1.3±0.1	8.0±0.2

Package VSOF5 (EMP5) (mm)

Symbol	A	B	D0	D1	E	F	P0	P1	P2	t	K	W
Dimension	1.83±0.1	1.83±0.1	$1.5^{+0.1}_{-0}$	0.5±0.1	1.75±0.1	3.5±0.05	4.0±0.1	4.0±0.1	2.0±0.05	0.25±0.05	0.75±0.1	8.0±0.2

2)Dimension of reel

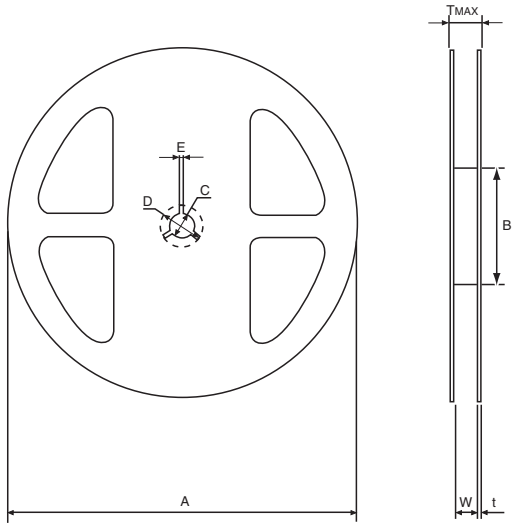


Fig.39

(mm)

Symbol	A	B	C	D	E	W	t	TMax.
Dimension	180 Max.	60±2.0	13.0±0.5	20.2 Min.	1.5 Min.	9.0±0.3	Label side(1.0) Back side(1.2)	17.4

3)Standard packaged quantity and IC direction

The standard packaged quantity is 3,000 pcs/reel. Orders should be in multiples of the standard packaged quantity. The ICs are TR oriented (as shown below).

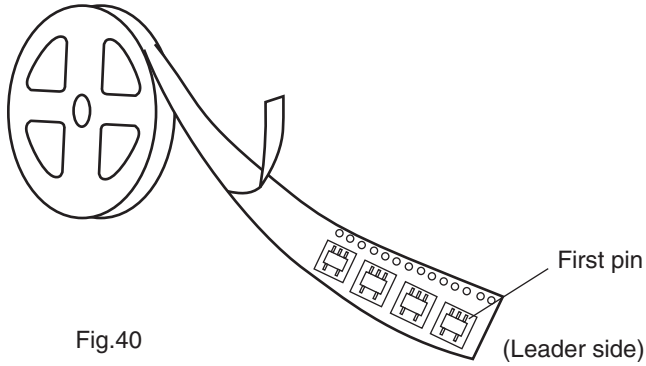
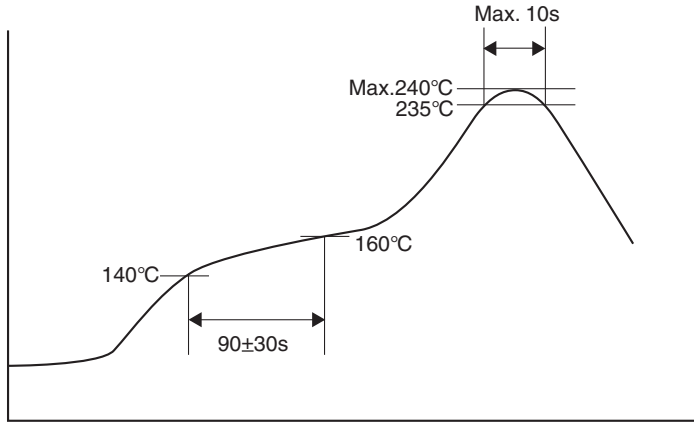


Fig.40

● Recommended mounting conditions

- SSOP5(SMP5C2) allows either reflow or flow soldering mounting.
- VSOF5(EMP5) allows reflow mounting. The mounting conditions are shown below.

1)Reflow



Up to two reflows are allowed.

Fig.41

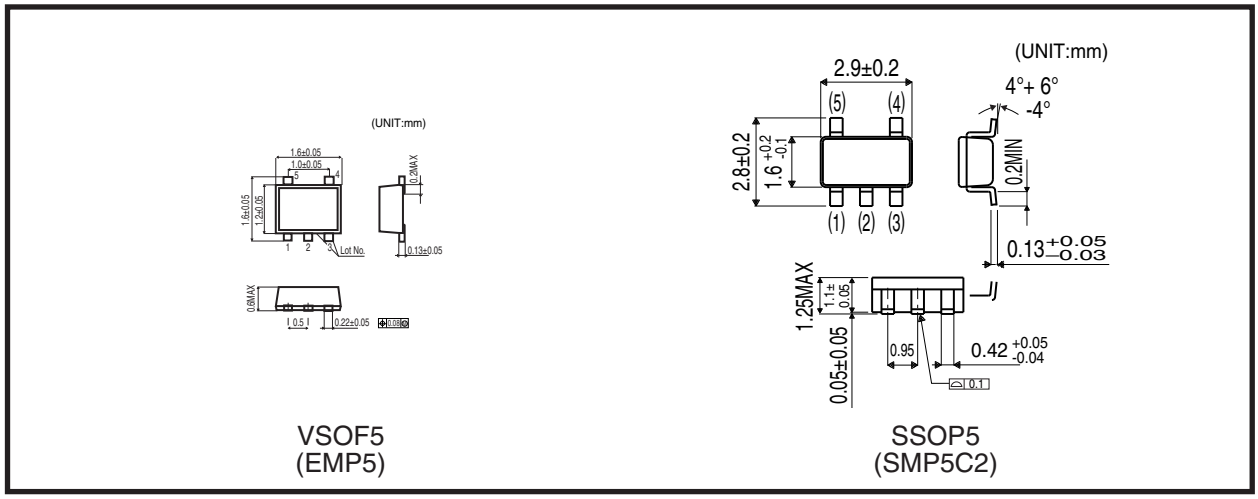
2)Flow soldering

Treatment process	Condition	
	Temperature	Time
Preheating section	150±10℃	60 to 120s
Solder bath	Max. 260℃	Max. 10s

3)Product storage conditions

Store the products in an environment of 5 to 30℃ in temperature and 70% RH or lower in humidity.

●Dimension



VSOF5
(EMP5)

SSOP5
(SMP5C2)

●Reference land pattern

VSOF5
(EMP5)

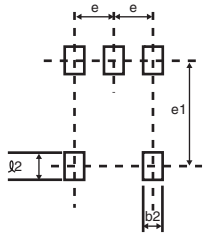


Fig.42

Unit:mm

Lead pitch e	Lead pitch e1	Land length ℓ2	Land width b2
0.50	1.35	0.35	0.25

SSOP5
(SMP5C2)

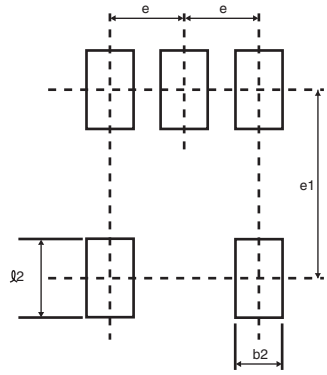


Fig.43

Unit:mm

Lead pitch e	Lead pitch e1	Land length ℓ2	Land width b2
0.95	2.40	1.00	0.60

For actual designing, take the board density, mountability, dimension tolerance, etc. for optimization.

●Part number and marking of samples

The BD52XX and BD53XX series products allow optimum selection of detection voltage, output circuit type and package according to the application.

Part No.

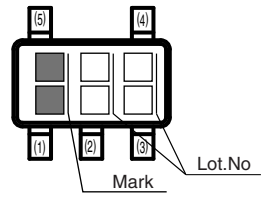
B D 5 X X X X

① ② ③

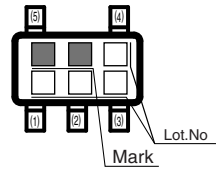
Part No.	Specification	Contents
①	Output circuit type	2 : Open drain output 3 : CMOS output
②	Detection voltage	Ex : V_{DET} : described in each 0.1V step for 2.3V to 6.0V range (29 means 2.9V)
③	Package	G : SSOP5 (SMP5C2) FVE : VSOF5 (EMP5)

Marking	Voltage	Part No.	Marking	Voltage	Part No.	Marking	Voltage	Part No.	Marking	Voltage	Part No.
PW	6.0V	BD5260	PB	4.1V	BD5241	RW	6.0V	BD5360	RB	4.1V	BD5341
PV	5.9V	BD5259	PA	4.0V	BD5240	RV	5.9V	BD5359	RA	4.0V	BD5340
PU	5.8V	BD5258	MV	3.9V	BD5239	RU	5.8V	BD5358	QV	3.9V	BD5339
PT	5.7V	BD5257	MU	3.8V	BD5238	RT	5.7V	BD5357	QU	3.8V	BD5338
PS	5.6V	BD5256	MT	3.7V	BD5237	RS	5.6V	BD5356	QT	3.7V	BD5337
PR	5.5V	BD5255	MS	3.6V	BD5236	RR	5.5V	BD5355	QS	3.6V	BD5336
PQ	5.4V	BD5254	MR	3.5V	BD5235	RQ	5.4V	BD5354	QR	3.5V	BD5335
PP	5.3V	BD5253	MQ	3.4V	BD5234	RP	5.3V	BD5353	QQ	3.4V	BD5334
PN	5.2V	BD5252	MP	3.3V	BD5233	RN	5.2V	BD5352	QP	3.3V	BD5333
PM	5.1V	BD5251	MN	3.2V	BD5232	RM	5.1V	BD5351	QN	3.2V	BD5332
PL	5.0V	BD5250	MM	3.1V	BD5231	RL	5.0V	BD5350	QM	3.1V	BD5331
PK	4.9V	BD5249	ML	3.0V	BD5230	RK	4.9V	BD5349	QL	3.0V	BD5330
PJ	4.8V	BD5248	MK	2.9V	BD5229	RJ	4.8V	BD5348	QK	2.9V	BD5329
PH	4.7V	BD5247	MJ	2.8V	BD5228	RH	4.7V	BD5347	QJ	2.8V	BD5328
PG	4.6V	BD5246	MH	2.7V	BD5227	RG	4.6V	BD5346	QH	2.7V	BD5327
PF	4.5V	BD5245	MG	2.6V	BD5226	RF	4.5V	BD5345	QG	2.6V	BD5326
PE	4.4V	BD5244	MF	2.5V	BD5225	RE	4.4V	BD5344	QF	2.5V	BD5325
PD	4.3V	BD5243	ME	2.4V	BD5224	RD	4.3V	BD5343	QE	2.4V	BD5324
PC	4.2V	BD5242	MD	2.3V	BD5223	RC	4.2V	BD5342	QD	2.3V	BD5323

BD52XG/BD53XXG
SSOP5 (SMP5C2)



BD52XXFVE/BD53XXFVE
VSOF5 (EMP5)



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The products listed in this document are designed to be used with ordinary electronic equipment or devices (such as audio visual equipment, office-automation equipment, communications devices, electrical appliances and electronic toys).
Should you intend to use these products with equipment or devices which require an extremely high level of reliability and the malfunction of with would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

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Products described herein are the objects of controlled goods in Annex 1 (Item 16) of Export Trade Control Order in Japan.
In case of export from Japan, please confirm if it applies to "objective" criteria or an "informed" (by MITI clause) on the basis of "catch all controls for Non-Proliferation of Weapons of Mass Destruction.