MAXIM

Single/Dual Very Fast TTL Output Comparators

General Description

The MAX9686 (Single) and MAX9698 (Dual) are very fast TTL comparators manufactured with a high frequency bipolar process (f_T = 6GHz) that are capable of very short propagation delays, yet maintain the excellent DC matching characteristics that are normally found only in slower comparators. The MAX9698 is a dual version of the MAX9686.

The MAX9686 is pin-comptabile with the LT1016 and Am686 but exceeds the AC characteristics of these devices.

The MAX9686 and MAX9698 have differential inputs and complementary outputs that are fully compatible with TTL logic levels. The extremely short propagation delays allow signal processing at frequencies in excess of 200MHz.

When the Latch Enable input goes high, the outputs go to the states defined by the input condition at the time of the latch transition. The outputs remain latched as long as the LE pin remains high. If the Latch Enable function is not used, the LE pin must be tied to ground.

Applications

High-Speed A/D Converters

High-Speed Line Receivers

Peak Detectors

Threshold Detectors

High-Speed Triggers

Features

- **6ns Propagation Delay**
- **2ns Latch Set-Up Time**
- **+5V, -5.2V Power Supplies**
- **Pin-Compatible to LT1016, Am686**
- **Available in Commercial and Military Versions**
- **Available in Small Outline**

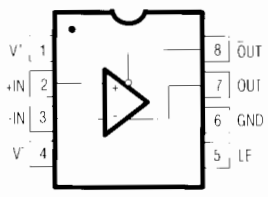
Ordering Information

PART	TEMP. RANGE	PACKAGE*
MAX9686CPA	0°C to +70°C	8 Lead Plastic DIP
MAX9686CJA	0°C to +70°C	8 Lead CERDIP
MAX9686CSA	0°C to +70°C	8 Lead Small Outline
MAX9686C/D	0°C to +70°C	Dice
MAX9686CTV	0°C to +70°C	8 Lead TO-99 Metal Can
MAX9686MJA	-55°C to +125°C	8 Lead CERDIP
MAX9686MTV	-55°C to +125°C	8 Lead TO-99 Metal Can
MAX9698CPE	0°C to +70°C	16 Lead Plastic DIP
MAX9698CJE	0°C to +70°C	16 Lead CERDIP
MAX9698CSE	0°C to +70°C	16 Lead Small Outline
MAX9698C/D	0°C to +70°C	Dice
MAX9698MJE	-55°C to +125°C	16 Lead CERDIP

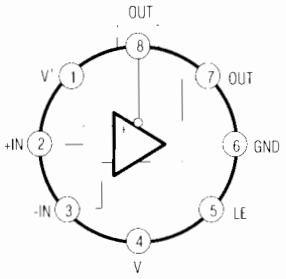
*Contact factory for availability of 20 Lead LCC

Pin Configurations

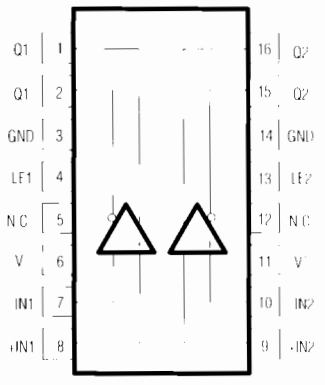
Top View



MAX9686
Plastic DIP, CERDIP, Small Outline



MAX9686
TO-99 Metal Can



MAX9698
Plastic DIP, CERDIP, Small Outline

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ABSOLUTE MAXIMUM RATINGS

Supply Voltages ..... ±6V
Power Dissipation (Notes 1,2) 336mW
Input Voltages ..... ±5V
Differential Input Voltages 3.5V
Output Current 20mA

Operating Temperature Range:
Commercial (MAX9686C/9698M) ..... 0 C to +70 C
Military (MAX9686M/9698M) ..... -55 C to +125 C
Storage Temperature Range ..... -55 C to +150 C
Lead Temperature (Soldering, 10 seconds) ..... 300 C

Note 1: Power derating above T_A = 70°C is based on a maximum junction temperature of 150°C and the following thermal resistance factors:

Package	θ_{JC}(°C/W)	θ_{JA}(°C/W)
DIP	75	180
SOIC	115	180
TO-99	115	150

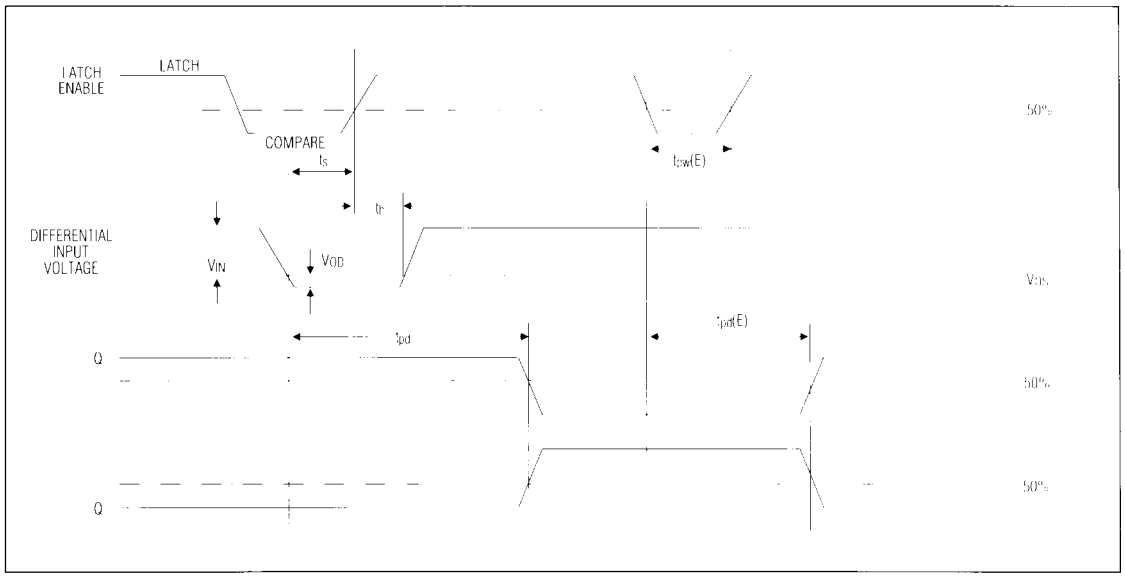
Note 2: Continuous short circuit protection is allowed to the following case and ambient temperatures: For MAX9698, continuous short circuit is allowed on one comparator at a time up to case temperatures of 85 C and ambient temperatures of 30 C.

Package	T_C(°C)	T_A(°C)
DIP	110	70
SOIC	95	70
TO-99	95	30

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_S = ±5V, T_A = 25°C unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX9686C/9698C MIN	MAX9686C/9698C TYP	MAX9686C/9698C MAX	MAX9686M/9698M MIN	MAX9686M/9698M TYP	MAX9686M/9698M MAX	UNITS
Input Offset Voltage	V_{OS}	R_S = 100Ω	-3		+3	-3		+3	mV
Temperature Coefficient	$\Delta V_{OS}/\Delta T$			4			4		µV/°C
Input Offset Current	I_{OS}				5.0			5.0	µA
Input Bias Current	I_B				25			25	µA
Common Mode Rejection Ratio	CMRR		80	96		80	96		dB
Power Supply Rejection Ratio	PSRR		70	85		70	85		dB
Input Voltage Range	V_{CM}		-3.0		+3.0	-3.0		+3.0	V
Latch Hi Input Voltage	V_{IH}		2.0			2.0			V
Latch Low Input Voltage	V_{IL}				0.8			0.8	V
Latch Low Input Current	I_{IL}	V_{LE} = 0V			-750			-750	µA
I/O Logic Levels Output High Voltage	V_{OH}	I_{OUT} = - 3mA	2.4	3.0		2.4	3.0		V
Output Low Voltage	V_{OL}	I_{OUT} = 8mA			0.5			0.5	V
Positive Supply Current (MAX9686) (MAX9698)	I_{CC}			16 32	25 50		16 32	25 50	mA
Negative Supply Current (MAX9686) (MAX9698)	I_{EE}			13 26	20 40		13 26	20 40	mA
SWITCHING CHARACTERISTICS (Each Comparator for MAX9698)									
Propagation Delays (guaranteed over full temperature range) Input to Output High	t_{pd+}	100mV pulse; 10mV overdrive		6.0	9		6.0	9	ns
Input to Output Low	t_{pd-}	100mV pulse; 10mV overdrive		5.7	8.5		5.7	8.5	ns
Propagation Delay Skew	$t_{pd+} - t_{pd-}$			0.3			0.3		ns
Latch Setup	t_S			2			2		ns



MAX9686 and MAX9698 Timing Diagram (worst case).

Application Information

Layout

Because of the large gain-bandwidth characteristic of the MAX9686 and MAX9698, special precautions need to be taken if the high speed capabilities of the devices are to be realized. A PC board with ground plane should be considered mandatory. All decoupling capacitors should be mounted as close as possible to the power supply pins. For low impedance applications microstrip layout at the input may be helpful. Close attention should be paid to the bandwidth of the decoupling and terminating components. Chip components to minimize lead inductance can be used as an advantage. An unused latch enable pin must be connected to ground.

Input Slew Rate Requirements

As with all high speed comparators, the high gain bandwidth product of these devices creates oscillation problems when the input traverses through the linear region. For clean switching without oscillation or steps in the output waveform, the input must meet certain minimum slew rate requirements. The tendency of the part to oscillate is a function of the layout and the source of impedance of the circuit employed. Both poor layout and larger source impedance will increase the minimum slew rate requirement.

Definition of Terms

V_{OS} Input Offset Voltage -- The voltage required between the input terminals to obtain zero volt differential at the output.

V_{IN} Input Voltage Pulse Amplitude.

V_{OD} Input Voltage Overdrive.

t_{pd+} Input to Output High Delay -- The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pd-} Input to Output Low Delay -- The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{pd+}(E)$ Latch Enable to Output High Delay -- The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output LOW to HIGH transition.

$t_{pd-}(E)$ Latch Enable to Output Low Delay -- The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition.

$t_{pw}(E)$ Minimum Latch Enable Pulse Width -- The minimum time the Latch Enable signal must be LOW to acquire and hold an input signal.

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t_S Minimum Set-up Time -- The minimum time, before the positive transition of the Latch Enable pulse, that an input signal must be present to be acquired and held at the outputs.

t_H Minimum Hold Time -- The minimum time, after the positive transition of the Latch Enable signal, that an input signal must remain unchanged to be acquired and held at the output.

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