Features

- **1024 x 1024 Pixels with Memory Zone**
- **Up to 60 Images/Second**
- **Built-in Antiblooming Device Providing an Electronic Shutter Function**
- **Pixel: 14 µm x 14 µm**
- **Image Zone: 14.34 x 14.34 mm²**
- **Four Outputs (256 x 1024 pixels) at 20 MHz Each**
- **Possible Binning 2 x 2**
- **Optical Shield against Parasitic Reflexions and Stray Light**
- **A/R Window in 400 - 700 nm Bandwidth**

Description

The TH7887A is especially designed for high data rate applications (up to 60 pict/s) in medical and industrial fields.

This area array image sensor consists of a 1024 x 1024 pixels (14 µm x 14 µm) image zone associated to a memory zone (masked with optical shield).

In order to increase data rate, the image zone is divided into four zones (256 x 1024 each) which are read in parallel through 4 different outputs (readout frequency up to 20 MHz/output leading to a total readout frequency of 80 MHz).

The TH7887A is designed with antiblooming gates.

Moreover, the 2 x 2 binning mode is available on this sensor. In this case, the image size is 512 x 512 with 28 µm x 28 µm pixels. Each output will read 128 x 512 pixels.

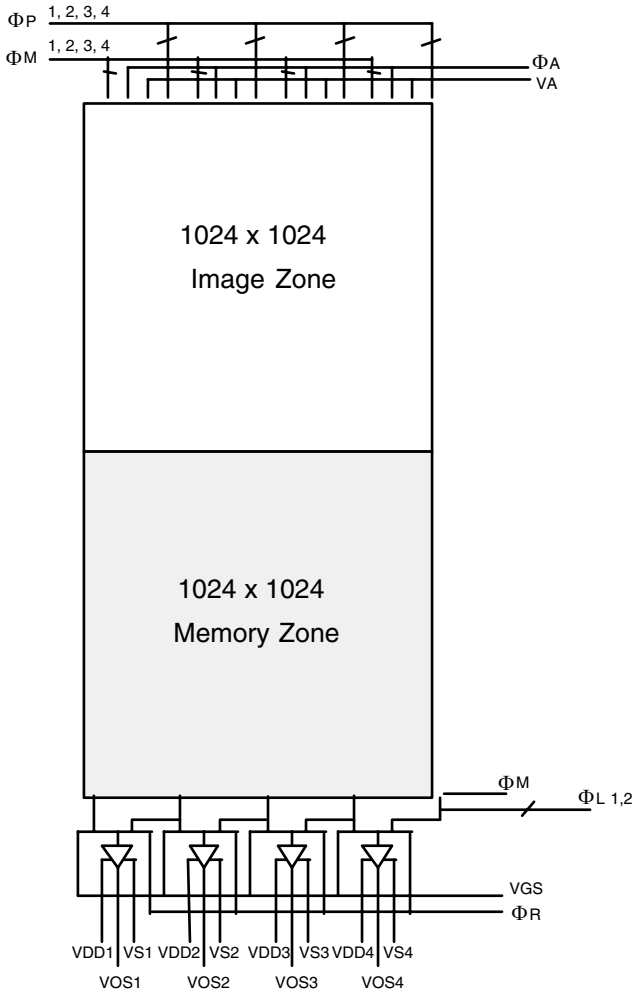
The TH7887A is sealed with a specific anti-reflective window optimized in 400 - 700 nm bandwidth.

Area Array CCD Image Sensor 1024 x 1024 Pixels with Antiblooming

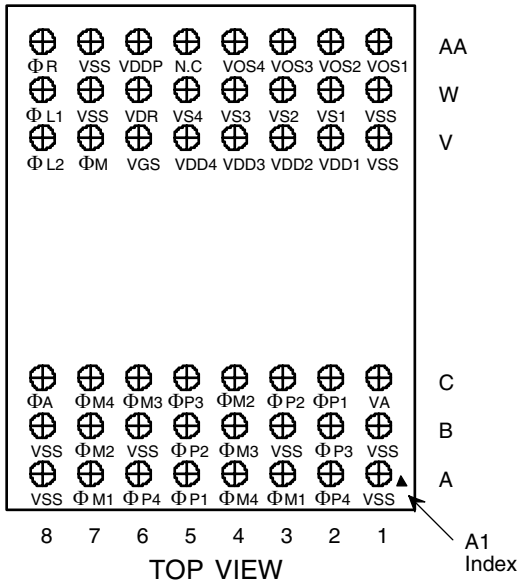
TH7887A

Rev. 2146A–IMAGE–05/02

Figure 1. TH7887A Organization



Pin Identification



Pin Number	Symbol	Designation
A2, A6[1]	ΦP4	Image zone clocks
B2, C5[1]	ΦP3	
B5, C3[1]	ΦP2	
A5, C2[1]	ΦP1	
A3, A7[1]	ΦM1	Memory zone clocks
B7, C4[1]	ΦM2	
B4, C6[1]	ΦM3	
C7, A4[1]	ΦM4	
V7	ΦM	Memory to register clock
W8	ΦL1	Readout register clocks
V8	ΦL2	
V2	VDD1	Output amplifier drain supply
V3	VDD2	
V4	VDD3	
V5	VDD4	
W2	VS1	Output amplifier source supply
W3	VS2	
W4	VS3	
W5	VS4	
AA6	VDDP	Screen voltage
AA5	NC	Not connected
V6	VGS	Register output gate bias

Pin Number	Symbol	Designation
AA1	VOS1	Video output signal
AA2	VOS2	
AA3	VOS3	
AA4	VOS4	
AA8	ΦR	Reset clock
C8	ΦA	Antiblooming gate clock
W6	VDR	Reset bias
C1	VA	Antiblooming diode bias
AA7, V1, W1	VSS	Substrate bias
W7, A8, B8	VSS	
B6, B1, A1, B3	VSS	

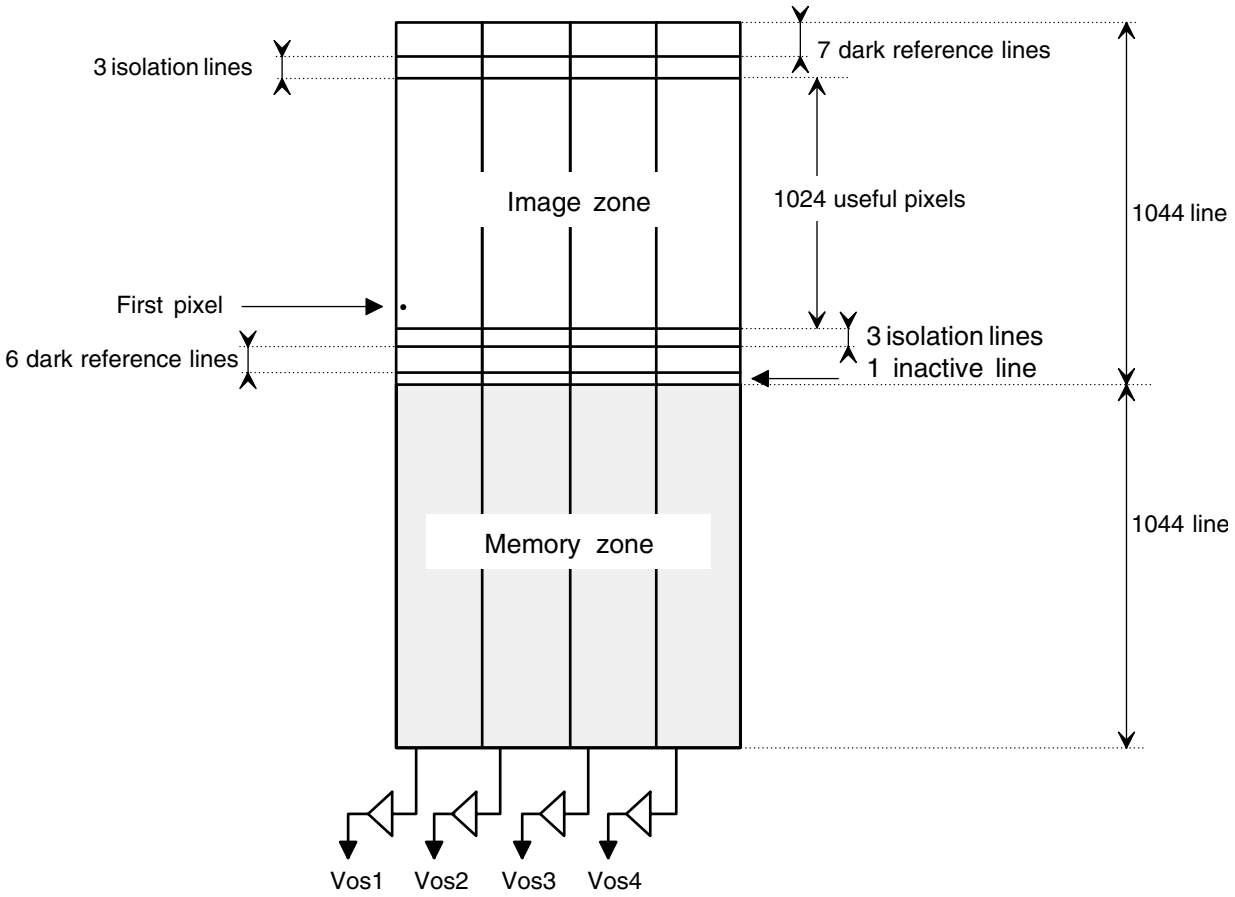
Note: 1. Short circuited on package.

Geometrical Characteristics

The image zone features 1024 useful lines (+ 20 extra lines) of 1024 pixels. For readout only, the full frame is split into 4 blocks of 256 columns.

The video line consists of 256 useful pixels, and 273 elements in total (for each output).

Figure 2. Video Line (on each output)



Pixels 1 to 17 : inactive prescan elements
Pixels 18 to 273 : useful elements

Figure 3. Pixel Layout

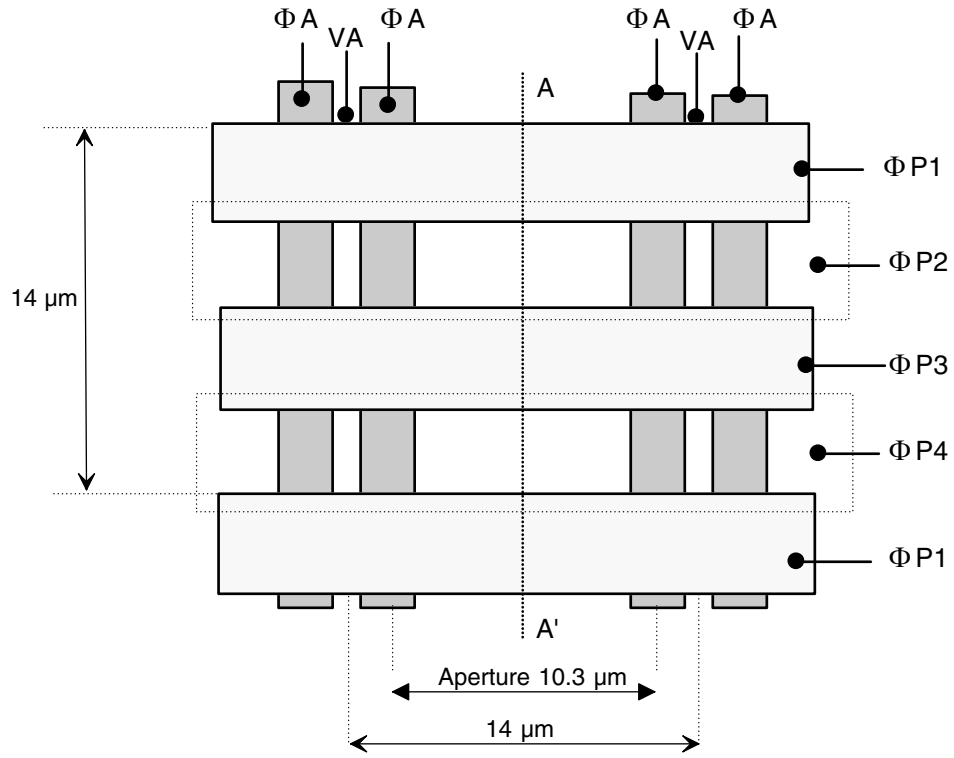
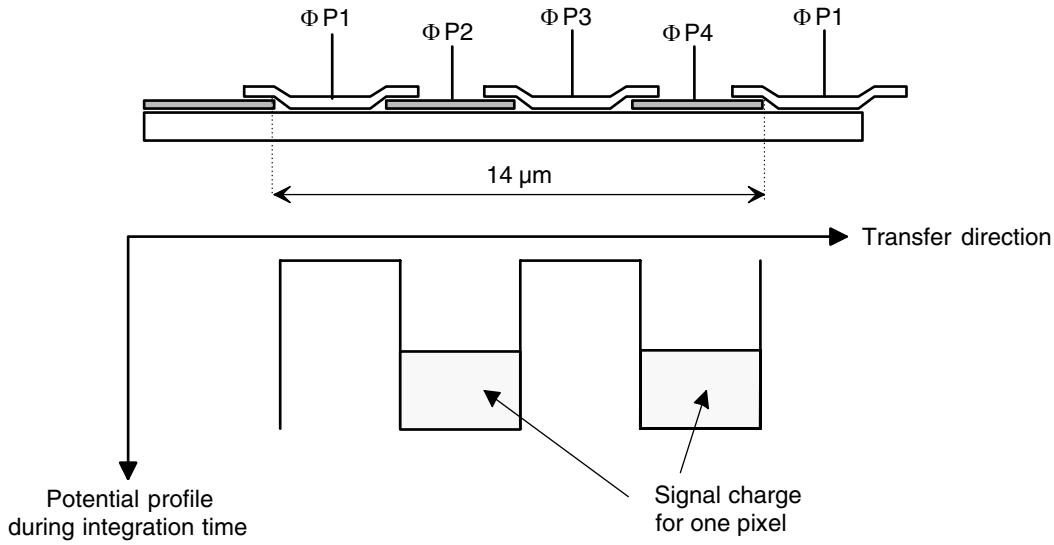


Figure 4. Cross-section AA’



Absolute Maximum Ratings*

Storage Temperature	-55°C to + 150°C
Operating Temperature	-40°C to + 85°C
Thermal Cycling	15°C/mm
Maximum Applied Voltages:	
A2, A6, B2, C5, B5, C3, A5, C2, A3, A7, B7, C4 B4, C6, C7, A4, V7, W8, V8, AA8, V6, AA5	-0.3V to 15V
V2, V3, V4, V5, W2, W3, W4, W5 W6, C1, AA6	-0.3V to 15.5V
C8	-0.3V to 12V
AA7, V1, W1, W7, A8, B8, B6, B1, A1, B3	Ground 0V

*NOTICE: Stresses above those listed under absolute maximum ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Range

The operating range defines the limits where function is guaranteed. Electrical limits of applied signals are given in the operating conditions section.

Operating Precautions

Shorting the video outputs to any other pin, even temporarily, can permanently damage the on-chip output amplifier.

Operating Conditions

Table 1. DC Characteristics

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Output amplifier drain supply	VDD1, VDD2, VDD3, VDD4	14.5	15	15.5	V
Screen voltage	VDDP	14.5	15	15.5	V
Reset bias	VDR	14.5	15	15.5	V
Antiblooming diode bias	VA	14.5	15	15.5	V
Register output gate bias	VGS	2.2	2.5	2.8	V
Output amplifier source supply	VS1,2,3,4	–	0	–	V
Ground	VSS	–	0	–	V

Timing Diagram

The following diagrams are given for:

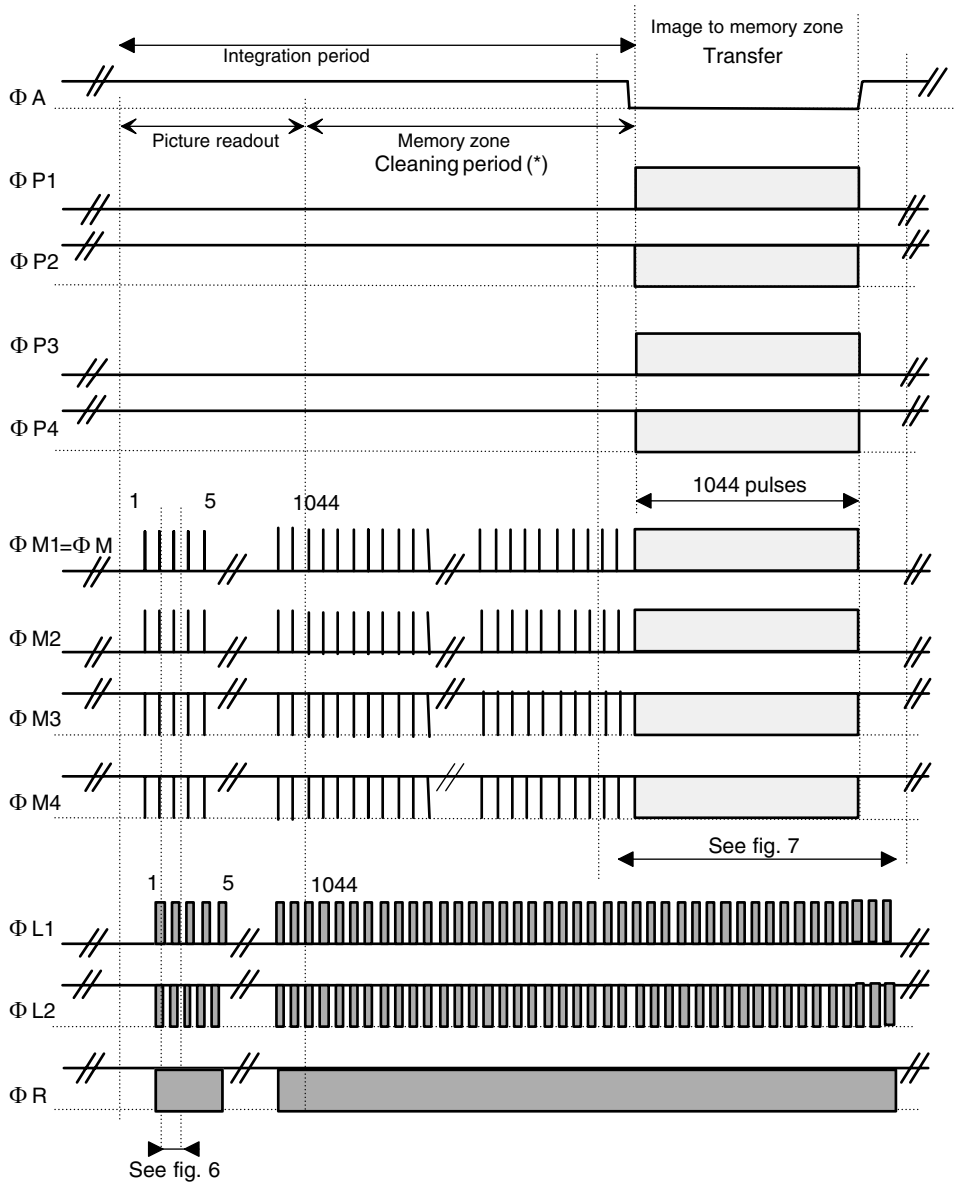
- 20 MHz readout frequency
- 1.25 MHz vertical transfer frequency

Readout of one image is performed in 2 steps:

- image zone to memory zone transfer
- memory zone to register transfer and readout of register

This last step is also an integration period, the duration of which can also be increased according to the required frame rates.

Figure 5. Frame Timing Diagram



(*) During the cleaning period, memory clocks must be pulsed as during readout time (specially for high temperature applications).

Figure 6. Line Timing Diagram

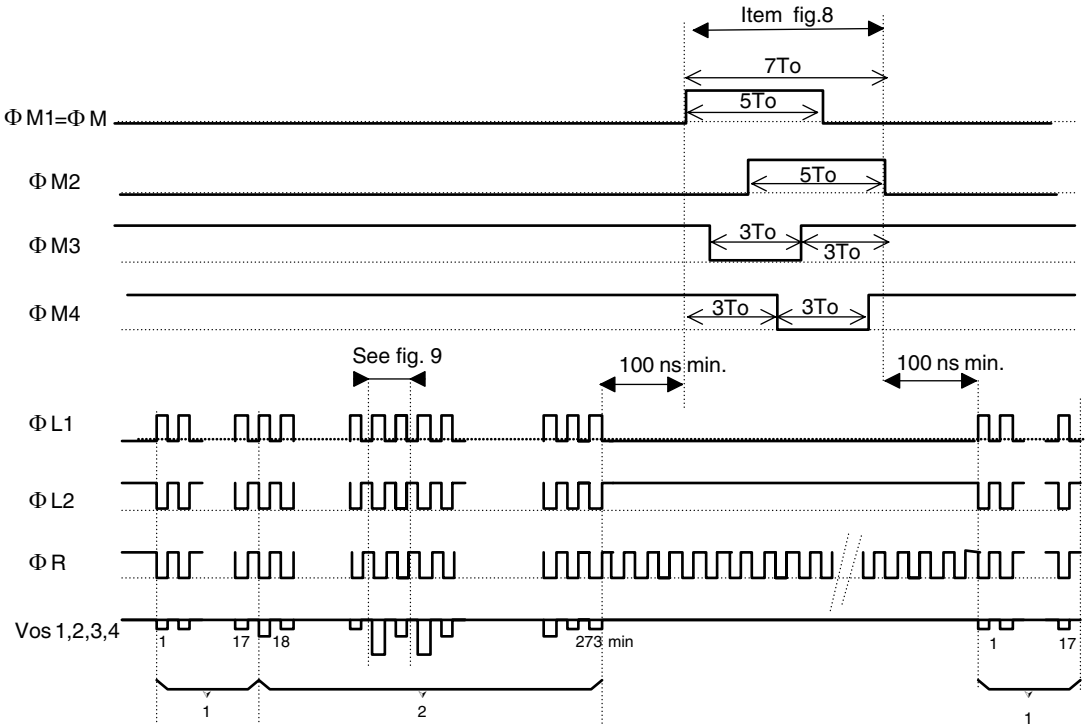


Figure 7. Vertical Transfer During Image to Memory Zone Transfer

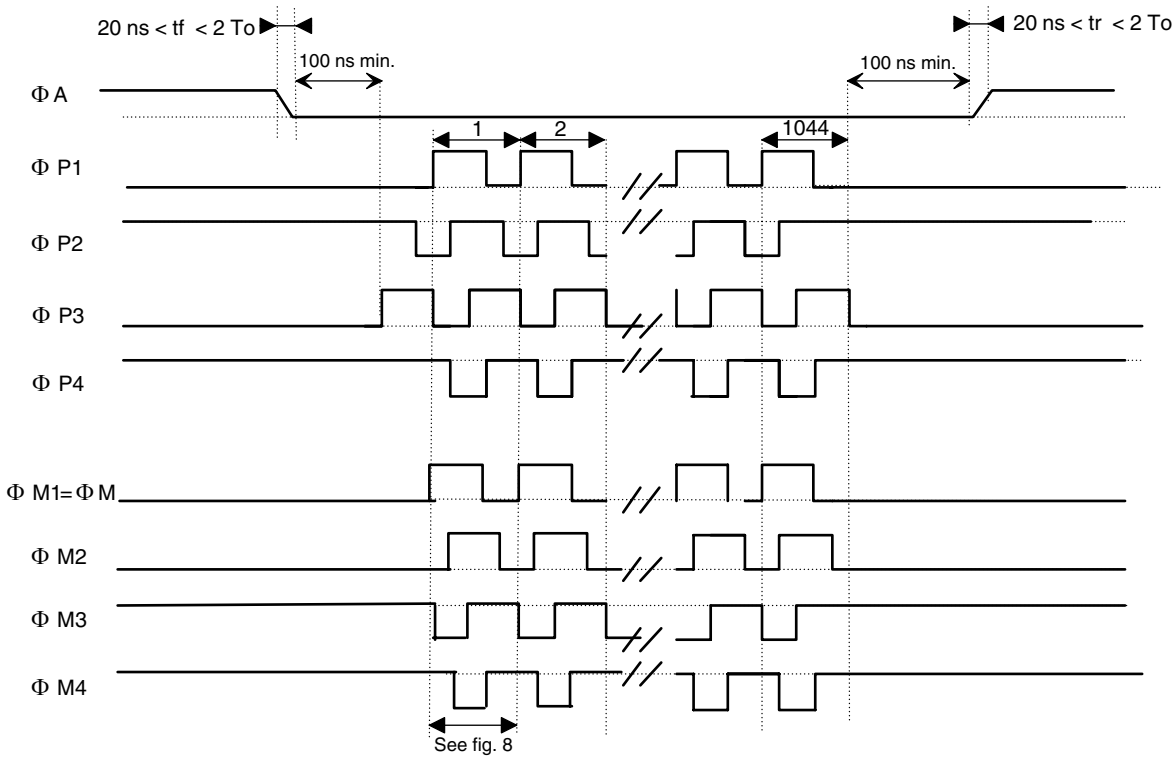


Figure 8. Transfer Period from Image Zone to Memory Zone (ΦP and ΦM) for 1.25 MHz Vertical Transfer Frequency (Fv = 1/Tv)

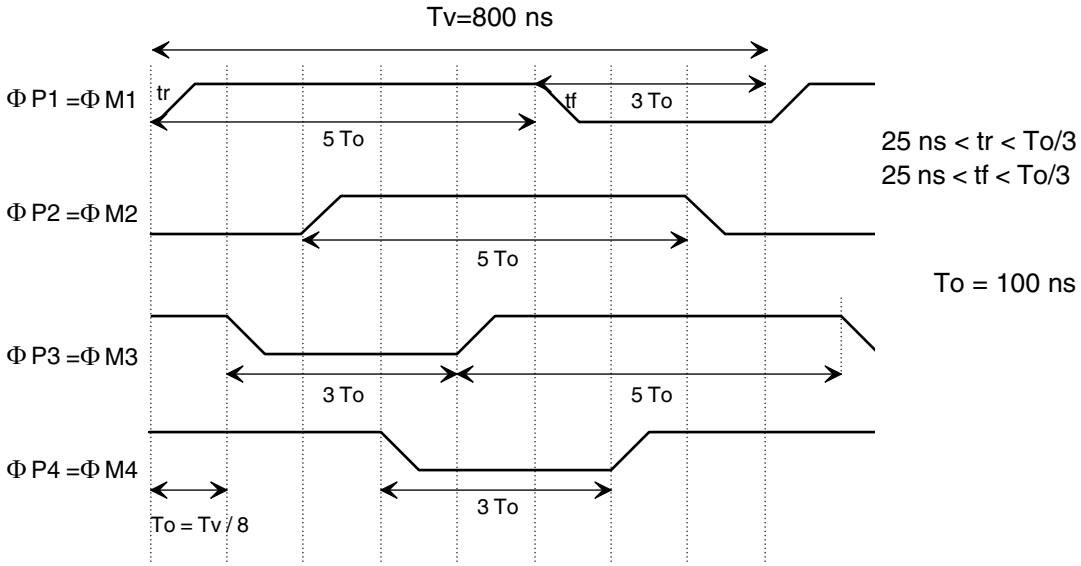
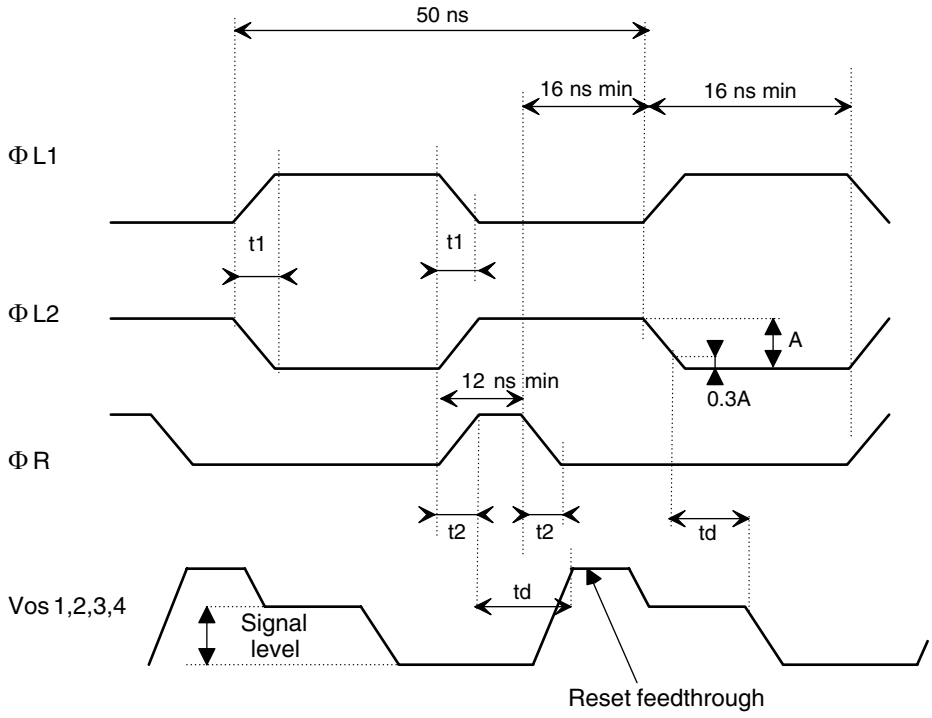


Figure 9. Output Diagram for Readout Register and Reset Clock 20 MHz Applications



t1 = 10 ns typ.
t2 = 5 ns typ.

td = 8 ns typical delay time

Cross over of complementary clocks (Φ L1, Φ L2) between 30% and 70% of maximum amplitude.

Binning Mode Operation

In this mode, the image is composed of 512 x 512 pixels (28 µm x 28 µm each).

Figure 10. Summation in the Readout Register of 2 Adjacent Lines.

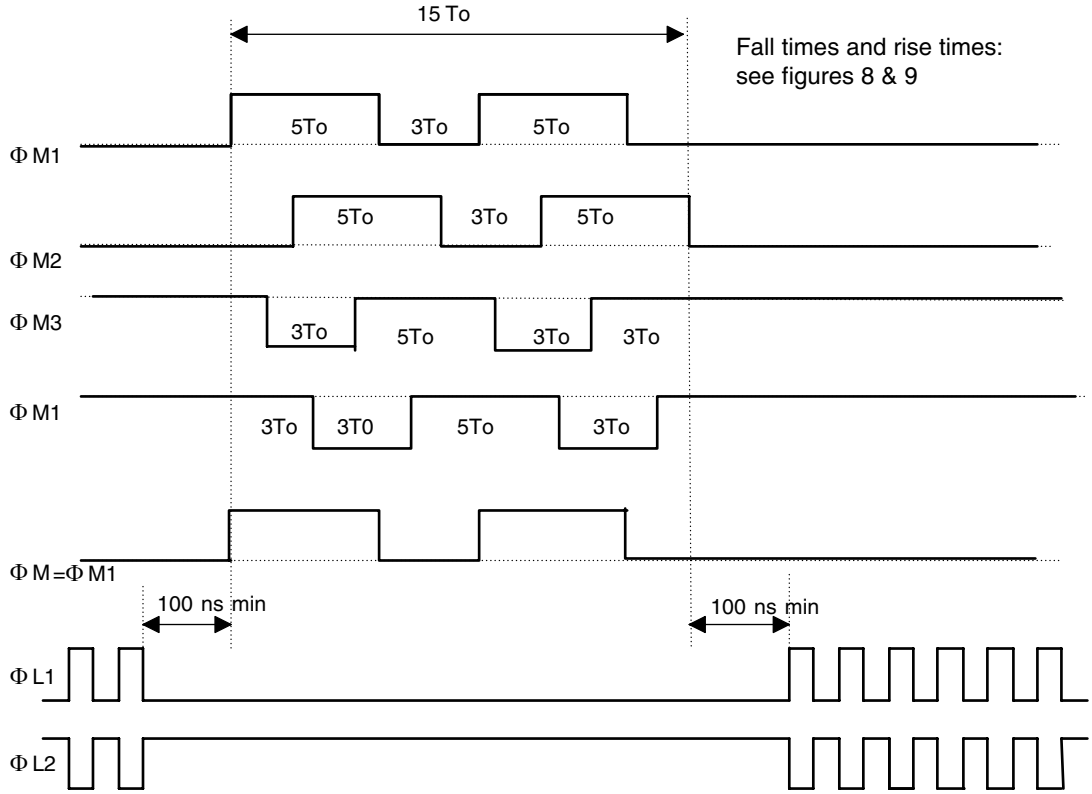
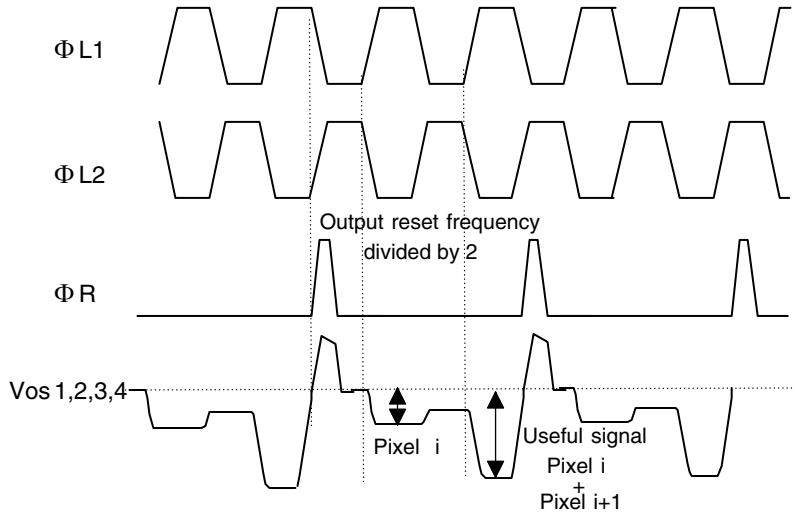


Figure 11. Summation of 2 Adjacent Pixels



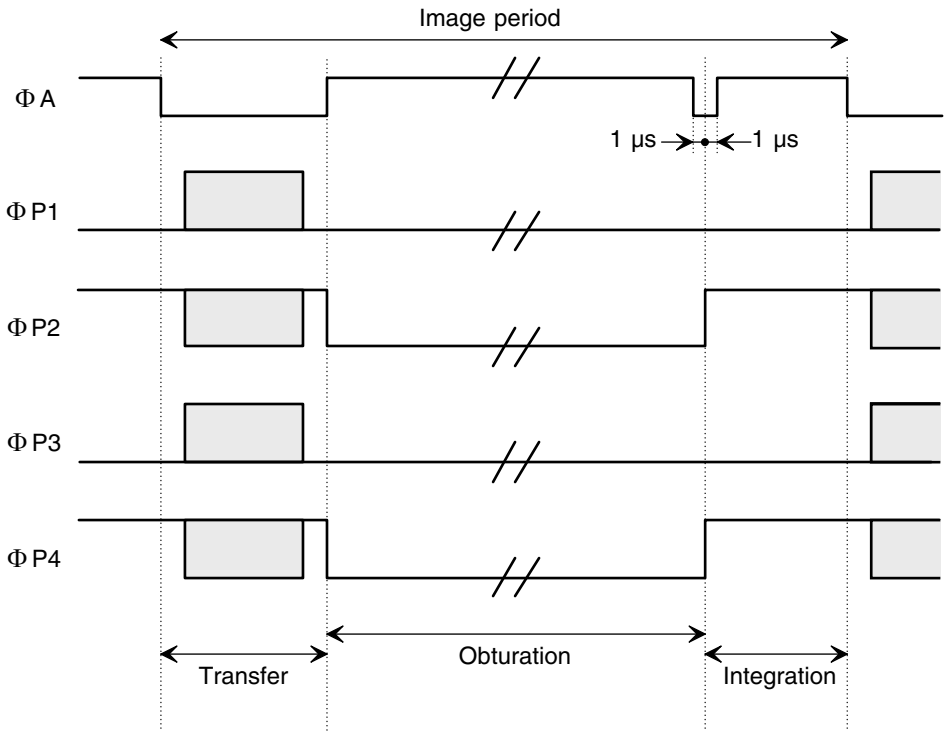
In binning mode operation maximum level of elementary pixel (14 x 14 µm) is reduced to Vsat/4.

Exposure Time Reduction

The TH7887A allows exposure time control (electronic shutter function).

The exposure time reduction is achieved by pulsing all the Φ Pi gates to 0V to continuously remove all photogenerated electrons through antiblooming drain VA.

Figure 12. Timing Diagram for Electronic Shutter



Fall times and rise times: see figures 7 & 8

Table 2. Drive Clock Characteristics

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Image zone clocks	ΦP1, 2, 3, 4					Typical input capacitance
High level		8.5	9	9.5	V	15 nF
Low level		0	0.5	0.8	V	See Figure 13
Memory zone clocks	ΦM1, 2, 3, 4					Typical input capacitance
High level		8.5	9	9.5	V	15.5 nF
Low level		0	0.5	0.8	V	See Figure 13
Memory to register clocks	ΦM					Typical input capacitance
High level		8.5	9	9.5	V	10 nF
Low level		0	0.5	0.8	V	
Antiblooming gate	ΦA					Typical input capacitance
High level (integration)		5.5	5.5	5.5	V	14 nF
Low level (transfer)		0	0.5	0.8	V	See Figure 13 and Figure 15

Table 2. Drive Clock Characteristics (Continued)

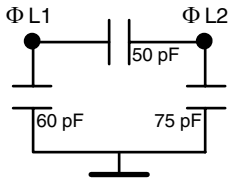
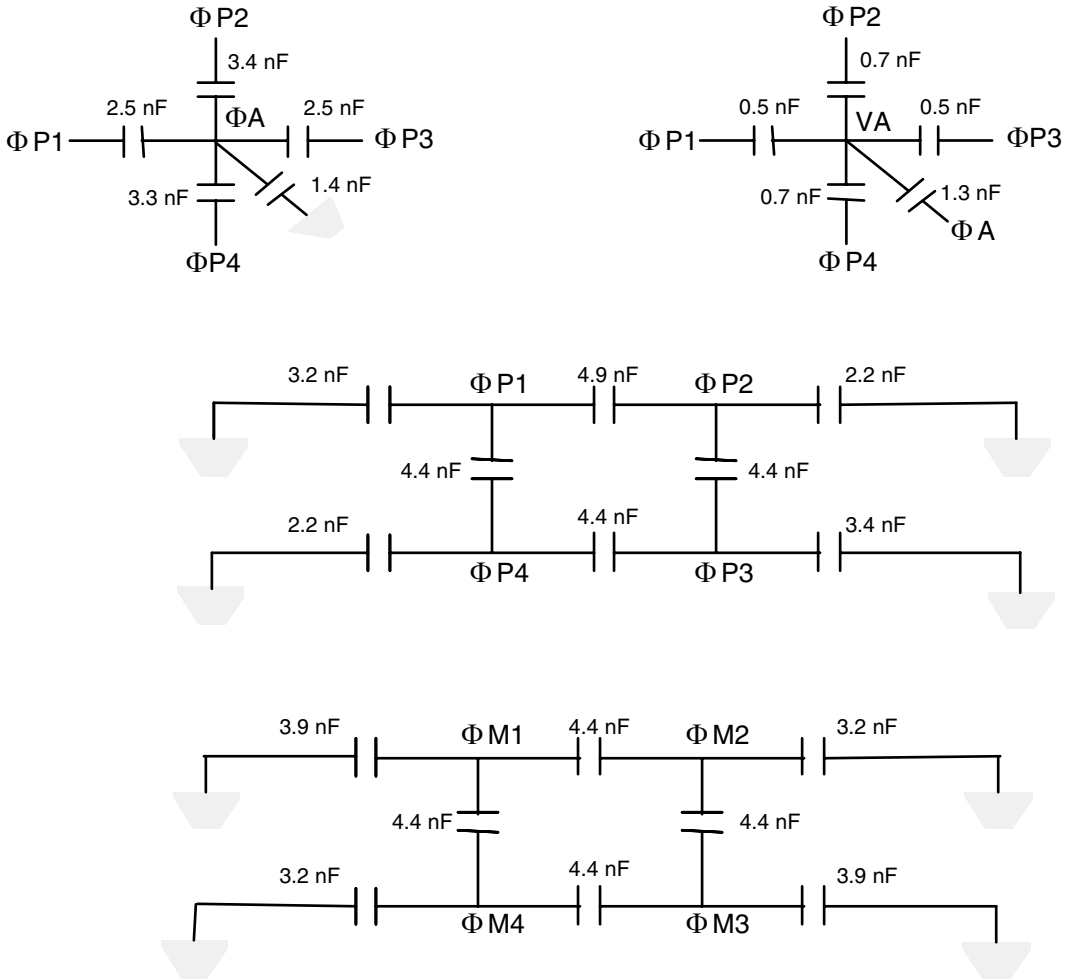
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Reset gate	ΦR					Typical input capacitance
High level		10	11	12	V	10 pF
Low level		0	0.5	0.8	V	
Readout register clocks	ΦL1, 2					
High level		8.5	9	9.5	V	
Low level		0	0.5	0.8	V	
Maximum readout register frequency	ΦF_H	–	20	23	MHz	See Figure 9
Image zone to memory zone transfer frequency	ΦF_V	–	1.25	1.7	MHz	See Figure 14

Figure 13. Capacitance Network for Drive Clocks



Electrical Performances

Table 3. Static and Dynamic Electrical Characteritics

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Output amplier supply current	I_{DD}	–	8.5	–	mA	per amplifier
Output impedance	Z_S	200	225	250	Ω	
DC output level	V_{REF}	–	11.5	–	V	
Output conversion factor	CVF	7.8	8	8.2	µV/ e-	

Electro-optical Performances

- General test conditions:
  - Top = 25°C (package back temperature).
  - Light source: 2854K with 2 mm BG38 filter (unless specified) + F/3.5 optical aperture.
  - 60 images per second mode (unless specified).
  - Typical operating conditions.
- Readout on each output.
- Measurements exclude dummy elements and blemishes.

Table 4. Electro-Optical Performance Characteristics

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Saturation output level	V_{SAT}	1.6	2	2.4	V	(1)
Responsivity at 640 nm Responsivity with BG38 filter	R	7 –	8 12	– –	V/µJ/cm^2 mV/lux	
Quantum efficiency at 640 nm	QE	–	14	–	%	See Figure 17
Gain dispersion between outputs	ΔG	–	1	2	%	
Photo response non-uniformity (1σ)	PRNU	–	1.3	1.7	% VOS	
Dark signal non-uniformity (1σ)	DSNU	–	0.14	0.2	mV	(2)
Average dark signal	V_{DS}	– –	1 2	1.5 2.8	mV mV	(3) (4)
Temporal RMS noise in darkness (Last line)	V_N	–	200	–	µV	(5)
Dynamic range	D	–	80	–	dB	(6)

Table 4. Electro-Optical Performance Characteristics (Continued)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Horizontal modulation transfer function at 500 nm	MTF	–	70	–	%	(7)
Vertical charge transfer inefficiency	VCTI	–	–	2.10^{-5}		(8)
Horizontal charge transfer inefficiency	HCTI	–	–	7.10^{-5}		(9)

Notes:
1. Pixel saturation (full well) as a function of vertical transfer frequency (see Figure 14) and antiblooming adjustment (see Figure 15).
2. After subtraction of dark signal slope due to memory readout time.
3. First line level referenced from inactive prescan elements (17 samples).
4. Last line level referenced from inactive prescan elements(17 samples).
5. Measured with Correlated Double Sampling (CDS) including 160 µV readout noise and dark current noise in the general test conditions.
6. Saturation to RMS noise in darkness ratio.
7. At Nyquist frequency.
8. VSAT/2 measurement and 1.25 MHz vertical transfer frequency.
9. VSAT/2 measurement and 20 MHz horizontal transfer frequency.

Figure 14. Saturation Level by full well with antiblooming out (ΦA high = 0V) vs the Vertical Transfer Frequency

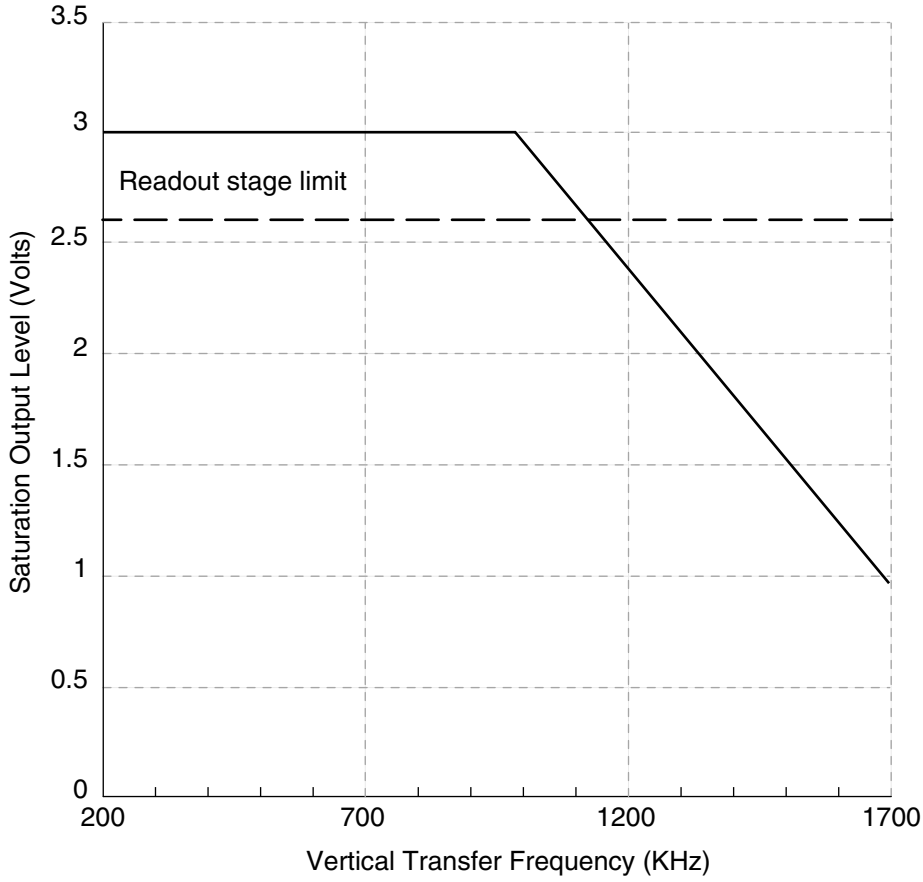


Figure 15. Saturation Level Limitation by the Antiblooming Effect on the Pixel

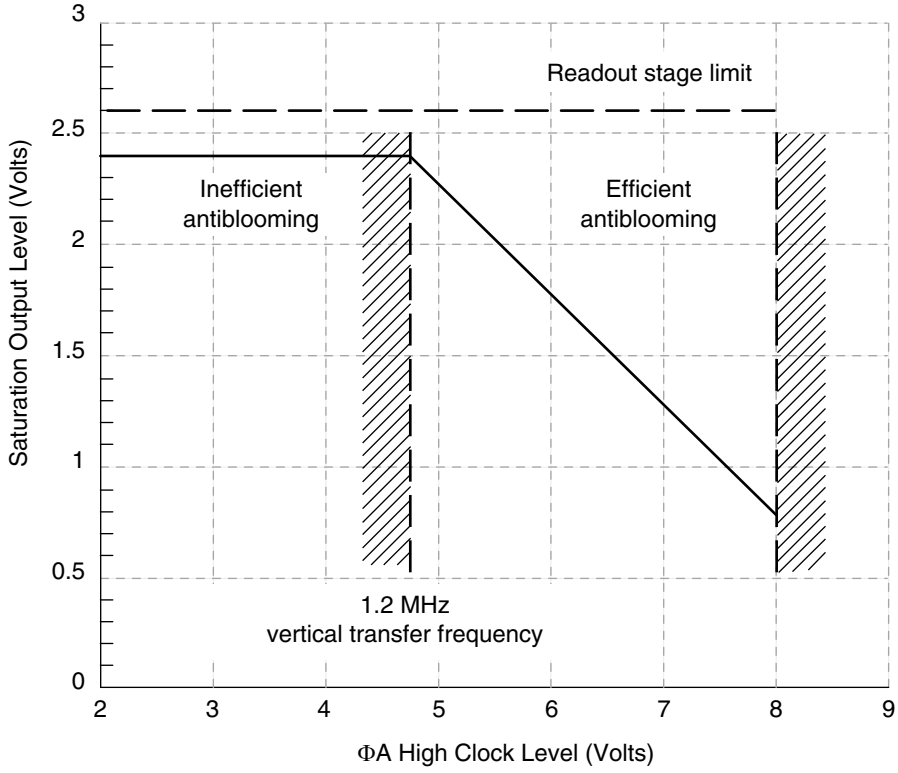


Figure 16. Smearing Effect

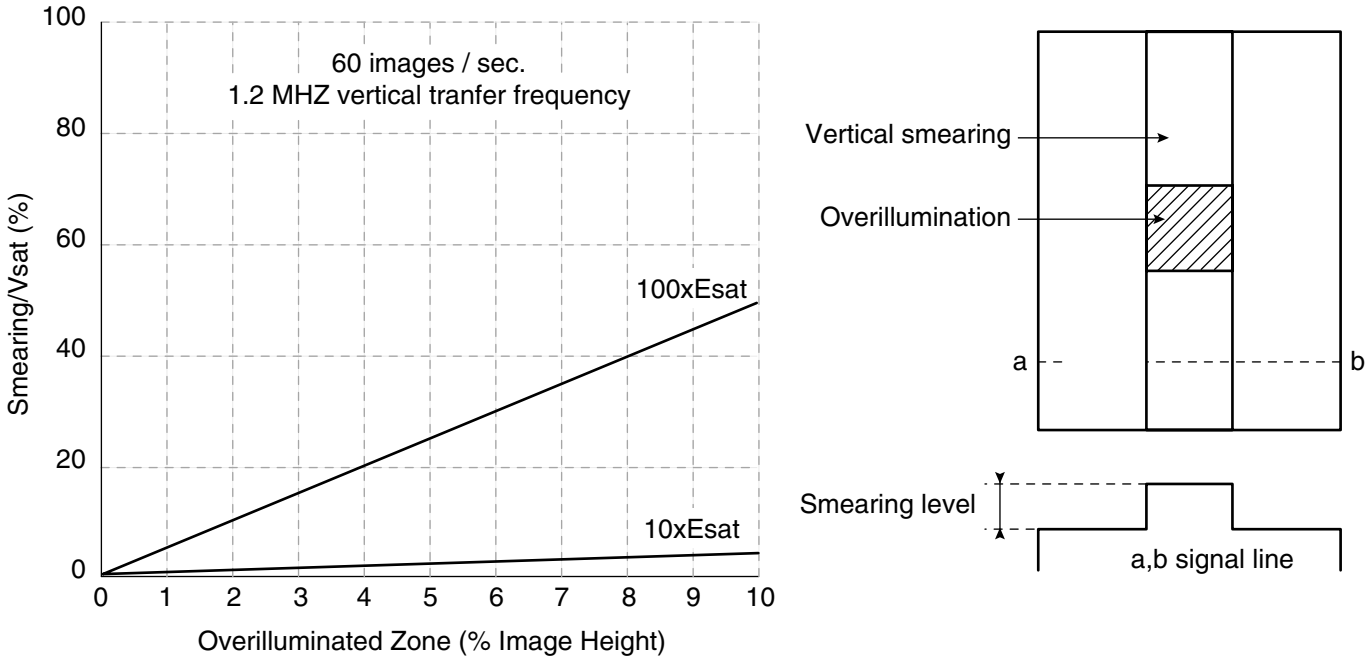


Figure 17. Spectral Response

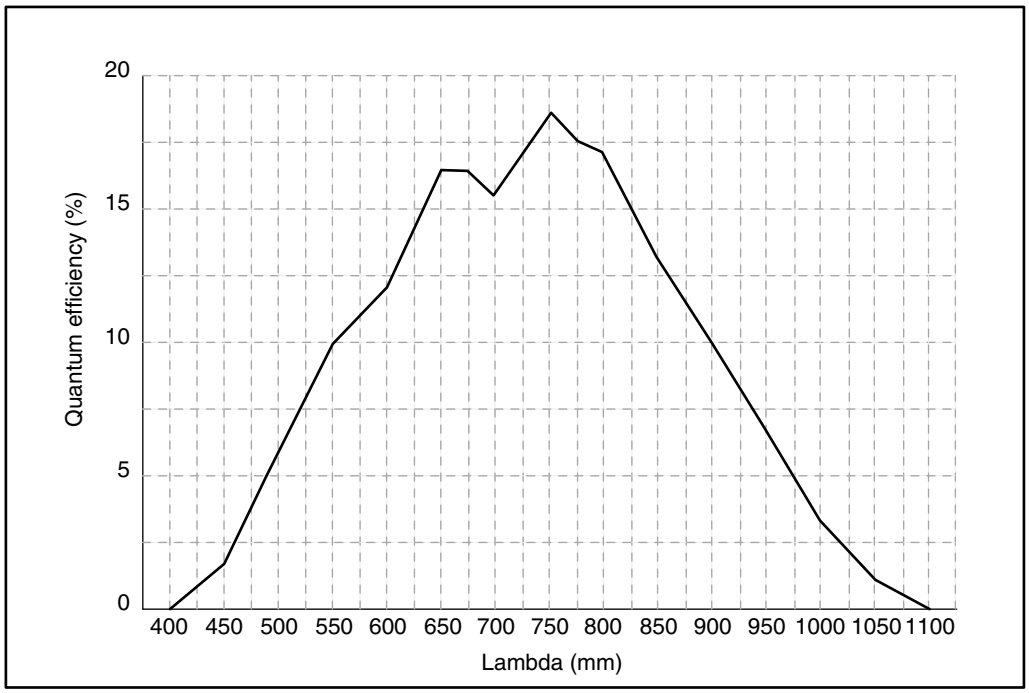


Image Quality Grade

Blemish

Max area of 2 x 2 defective pixels.

Clusters

Less than 7 contiguous defects in a column.

Columns

More than 7 contiguous defects in a column.

General Measurement Conditions

Room temperature	25°C
Frequency	60 images/second typical operating conditions
Considered image zone	1024 x 1024
Light source	2854 K with BG38 filter + F/3.5 optical aperture

Table 5. At V_{OS} = 0.7 Vsat.

Type	White	Black
Blemishes/clusters	α > 20% $\overline{Vos}_S$	$\lvert\alpha\rvert$ > 30% $\overline{Vos}$
Columns	α > 10% $\overline{Vos}$	$\lvert\alpha\rvert$ > 10% $\overline{Vos}$

Table 6. In darkness, T = 25°C, 60 images/second

Blemishes/clusters	α > 10 mV(1)
Columns	α > 5 mV(1)

Note: 1. Reference is Vo : average darkness signal

Number of Defects

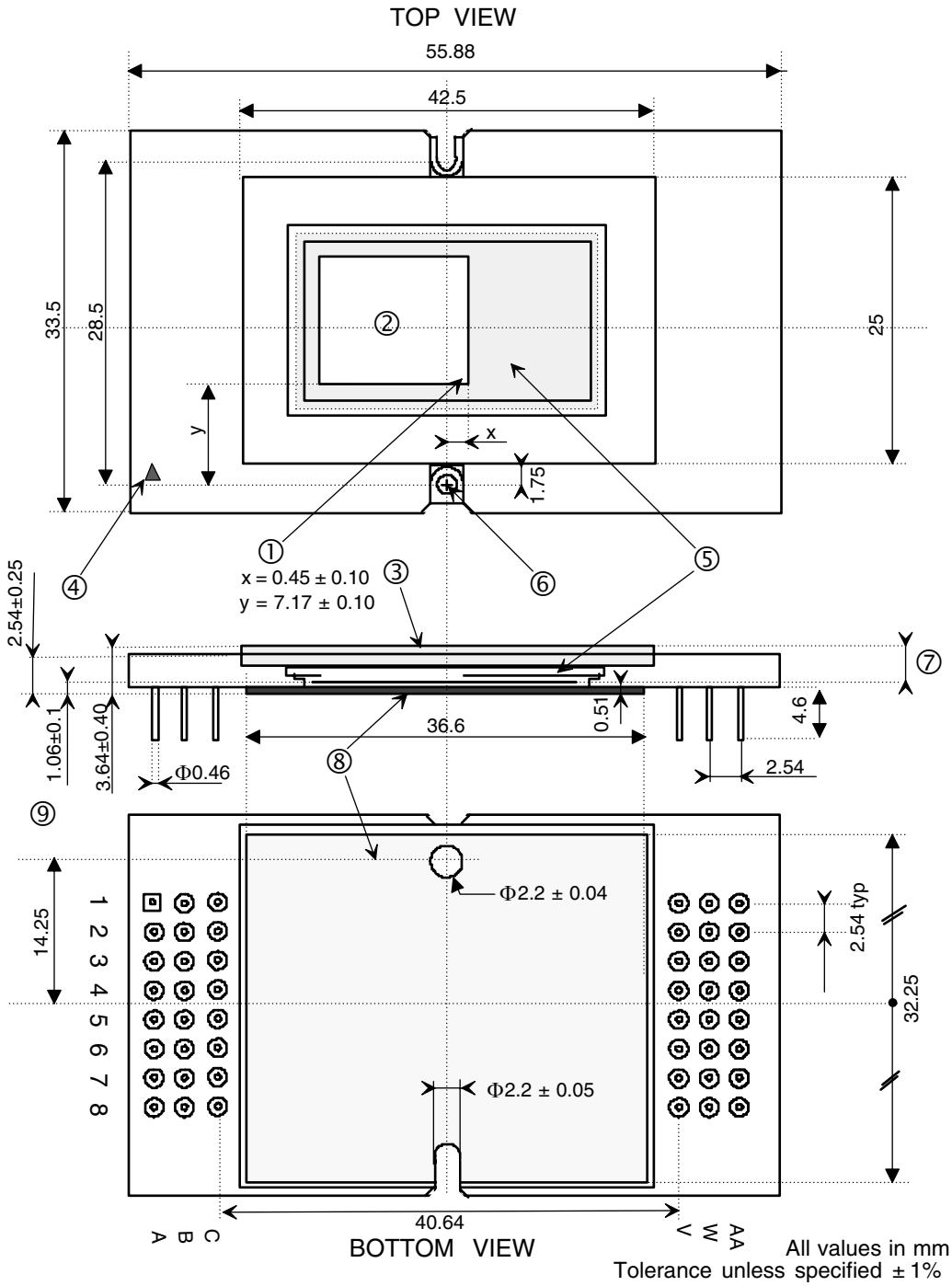
Total pixel number affected by blemishes and clusters	100
Maximum number of clusters	10
Maximum number of columns	5

α : amplitude of video signal of defect with respect to mean output voltage $\overline{Vos}$

Ordering Code

TH7887AVRH

Outline Drawing



① 1st useful pixel - readout through Vos1
② Photosensitive area
③ Glass window thickness: 1.5 ± 0.1 mm (antireflective coating with 400 - 700 nm transmission: 99%)
④ A1 index
⑤ Optical shield
⑥ Reference for first pixel position
⑦ Optical distance between photosensitive area and
- external face of the window: 1.93 ± 0.30 mm
- back side of the package: 1.71 ± 0.15 mm
⑧ Metal plate connected to VSS
⑨ Parallelism between CCD and back side has a maximum value of 100 µm

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