Features

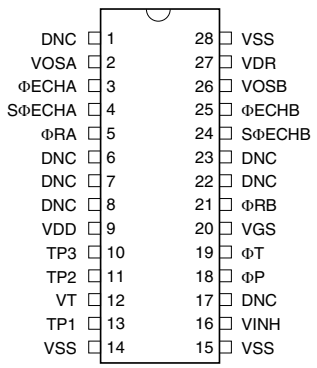
- **Pixel Size: 11 µm x 13 µm (13 µm Pitch)**
- **High Data Output Rate: 20 MHz**
- **High Responsivity and Resolution Over a Wide Spectral Range: from Blue (400 nm) up to Near Infrared (1,100 nm)**
- **Low Dark Signal and Improved Uniformity**
- **Low Temporal Noise and High Dynamic Range: Over 6000/1**
- **Ease and Flexibility of Operation:**
  - **Only Two External Basic Drive Clocks**
  - **Choice of Internal or External Sampling and Reset**
- **28-lead DIL Package**
- **Available with Standard Window or Antireflective Window in the Bandwidth 450 to 750 nm**

Linear CCD Image Sensor (2048 Pixels)

TH7841A

Pin Identification

Pin Number	Symbol	Designation
2	V_{OSA}	Video Output Signal A (Odd Channel)
3	Φ_{ECHA}	A Sample-and-hold Gate Input Channel
4	$S\Phi_{ECHA}$	A Internal Sampling Clock Output Channel
5	Φ_{RA}	A External Reset Clock Input Channel
9	V_{DD}	Output Amplifier Drain And Internal Logic Supply
10	TP3	Test Point 3
11	TP2	Test Point 2
12	VT	Register and Photosensitive Zone DC Bias
13	TP1	Test Point 1
14, 15, 28	V_{SS}	Substrate Bias (Ground)
16	V_{INH}	Internal Sampling Clock Inhibiting Input (Dc Bias)
18	Φ_P	Transfer Clock
19	Φ_T	Register Transport Clock
20	V_{GS}	Output Gate DC Bias
21	Φ_{RB}	B External Reset Clock Output Channel
24	$S\Phi_{ECHB}$	B Internal Sampling Clock Output Channel
25	Φ_{ECHB}	B Sample-and-hold Gate Input Channel
26	V_{OSB}	Video Output Signal B (Even Channel)
27	V_{DR}	Reset DC Bias
1, 6, 7, 8, 17, 22, 23	DNC	Do not Connect



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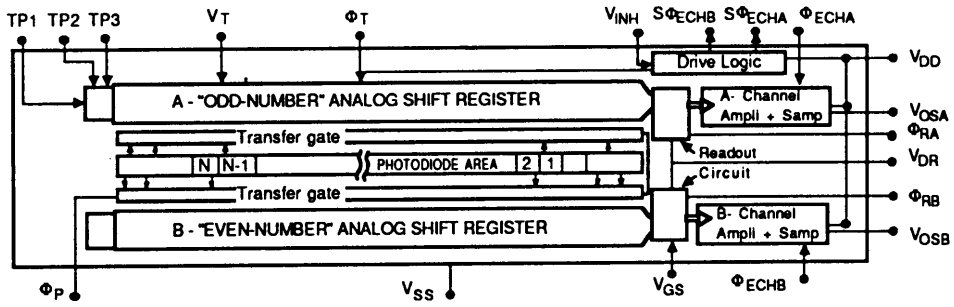


Absolute Maximum Ratings*

Storage Temperature	-55°C to +150°C
Operating Temperature	0°C to +70°C
Thermal Cycling	15°C/mn
Maximum Voltages:	
• Pins: 3, 5, 9, 10, 11, 13, 16, 19, 20, 21, 25, 27	-0.3V to +18V
• Pins: 12. 18	-0.3V to +16V
• Pins: 14, 15, 28	0V

*NOTICE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Range

Operating range defines the temperature limits between which the functionality is guaranteed: 0°C to 70°C.

Operating Precautions

Shorting the video output to V_{SS} to V_{DD}, even temporarily, can permanently damage the output amplifier.

Operating Conditions (T = 25°C)

Table 1. DC Characteristics

Parameter	Symbol	Values			Unit	Note
		Min	Typ	Max		
Output Amplifier Drain Supply	V_{DD}	14	15	16	V	
Reset DC Bias	V_{DR}	12	13	14.5	V	(1)
Output Gate DC Bias	V_{GS}	5.5	6	6.5	V	
Photosensitive Zone and Register DC Bias	V_T	6	6.5	7	V	(2)
Substrate Bias	V_{SS}	0.0	0.0			
Test Point 1	TP1		V_{DD}		V	(3)
Test Points 2 and 3	TP2, TP3		V_{SS}		V	(3)

Notes: 1. It is recommended to maintain V_{DR} at V_{DD} - 2V.

2. V_T nominal =

$$\frac{(V\Phi_T)\text{high} + (V\Phi_T)low}{2} \pm 5\%$$

3. No use for operation – For testing purpose only.

Basic Internal Configuration

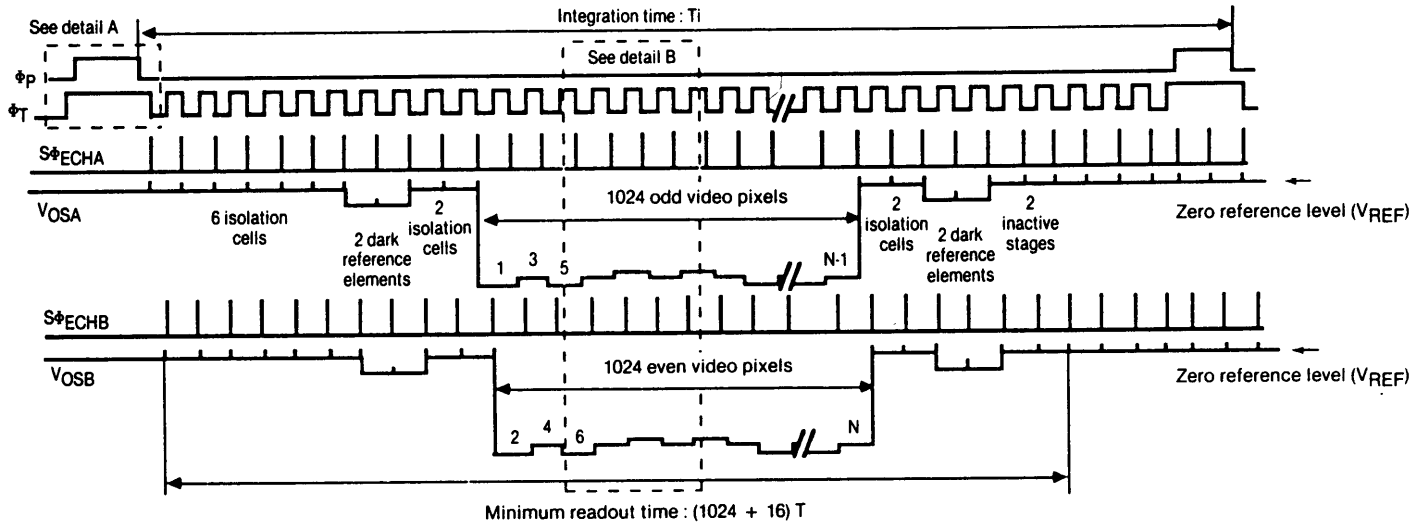
$S\Phi_{ECHA}$ and Φ_{RA} $S\Phi_{ECHB}$ and Φ_{RB}	internal to TH7841A

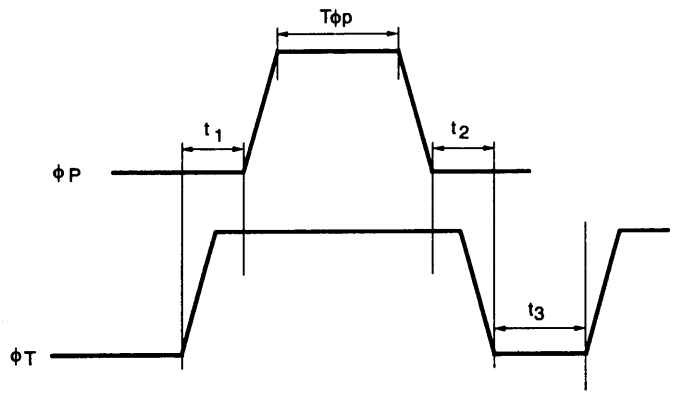
Table 2. Selection of Nominal Mode

Option	Implementation	Note
Internal Sampling	V_{INH} (16) Connected to V_{SS} $S\Phi_{ECHA}$ (4) and Φ_{ECHA} (3) Strapped $S\Phi_{ECHB}$ (24) and Φ_{ECHB} (25) Strapped	(1)
Internal Reset	Φ_{RA} (5) and Φ_{RB} (21) Connected to VDD	

Note: 1. Make the straps as short as possible to avoid any parasitic coupling to these connections. The load capacitance introduced by the strap should not exceed 5 pF.

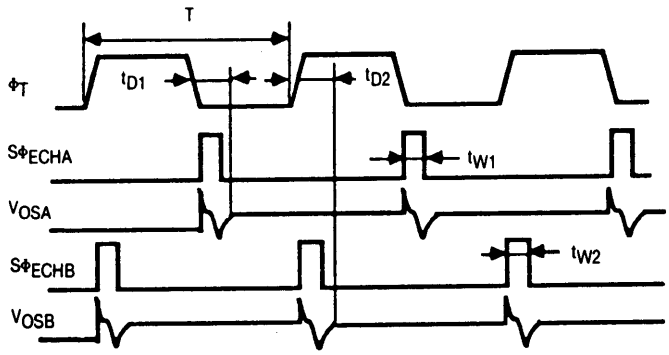
Figure 1. Timing Diagram — Clocks and Video Output Timing Diagram in Internal Sampling Mode





Detail A

$T_{\Phi P}$: Minimum value : 100 ns
Recommended 0.5 to 1 µs
t_1 and $t_3 > 0$ $t_2 >$ or < 0
Φ_P = pulse may end before or after Φ_T returns to the low level



Detail B

Φ_T : duty cycle : 50 ± 10 %
rise and fall time > 15 ns

$t_{W1} = t_{W2}$ = 30 ns typ.
$t_{D1} = t_{D2}$ = 50 ns typ.

Table 3. Drive Clock Characteristics (see Figure 1)

Parameter	Symbol	Logic	Values			Unit	Note
			Min	Typ	Max		
Transfer Clock	$\Phi_P\Phi_T$	High	12	13	14	V	(1)
Register Transport Clock		Low	0.0	0.4	0.6		
Register Transport Clock Capacitance	$C\Phi_T$			800	1200	pF	
Transfer Clock Capacitance	$C\Phi_P$			200	300	pF	

Note: 1. Transients under 0.0V in the clock pulses will lead to charge injection, causing a localized increase in the dark signal if such spurious negative transients are present, they can be suppressed by inserting a serial resistor of appropriate value (typically 20 to 100Ω) in the corresponding driver output.

Table 4. Static and Dynamic Electrical Characteristics

Parameter	Symbol	Values			Unit	Note
		Min	Typ	Max		
DC Output Level	V_{REF}	8	10	12	V	
Output Impedance	Z_S		500		Ω	
Register Single-stage Transfer Efficiency	CTE	99.992	99.998		%	V_{OS} = 1V(1)
Max. Data Output Frequency	F_S max.	12	20		MHz	(2)
Input Current on Pins: 3, 5, 10,11,12, 13, 18, 19, 20, 21, 25	Ie			2	µA	Ve = 15V All other pins: 0V
Peak Current Sink on Φ_T Clock	$(I\Phi_T)_P$		500		mA	t_{rise} = 15 ns
Peak Current Sink on Φ_P Clock	$(I\Phi_P)_P$		125		mA	t_{rise} = 15 ns
Output Amplifier Drain Supply Current	I_{DD}		17		mA	V_{INH} = 0V V_{DD} = 15V
Static Power Dissipation	P_D		255	300	mW	V_{INH} = 0V V_{DD} = 15V

Notes: 1. V_{OS} = average video output voltage. Measurement excludes first and last pixels.
2. $F_S = 2F\Phi_T$. The minimum clock frequency is limited by the increase in dark signal.

Electro-optical Performance

General measurement conditions: T_C = 25°C; T_i = 1 ms; $F\Phi_T$ = 2.5 MHz.

Light source: tungsten filament lamp (2854 K) + BG 38 filter (2 mm thick) + F/3.5 aperture. The filter limits the spectrum to 700 nm; in these conditions, 1 µJ/cm^2 corresponds to 3.5 lux.s.

Typical operating conditions; internal clock mode (see Table 2).

First and last pixels, as well as reference elements, are excluded from the specification.

Measurements taken on each output in succession.

Table 5. Electro-optical Performance

Parameter	Symbol	Values			Unit	Note
		Min	Typ	Max		
Saturation Output Voltage	V_{SAT}	1.3	1.8	2.2	V	(1)(2)
Saturation Exposure	E_{SAT}		0.33		µJ/cm^2	
Responsivity	R	2.5	2.9		V/µJ/cm^2	
Responsivity Unbalance	ΔR/R		2	8	%	(3)
Photo-response No-uniformity Peak-to-peak	PRNU		±5	±10	% V_{OS}	V_{OS} = 50 mV to 1V
Contrast Transfer Function at FN (38 l p/mm)	CTF		70		%	V_{OS} = 0.75V
Temporal Noise in Darkness			160		µVrms	(4)
Dynamic Range (Relative to rms Noise)	DR	3000	6000			
Average Dark Signal	V_{DS}		0.08	0.5	mV	(1)
Dark Signal Non-uniformity	DSNU		0.15	0.5	mV	

Notes:
1. Value measured with respect to zero reference level (see Figure 1).
2. Conversion factor is typically 1.1 µV/e-.
3. ΔR/R is defined as

$$\frac{200|RA - RB|}{RA + RB}$$

where RA is responsivity of video output A
RB is responsivity of video output B
4. Measured in Correlated Double Sampling (C.D.S.) mode.

Figure 2. Typical Spectral Response

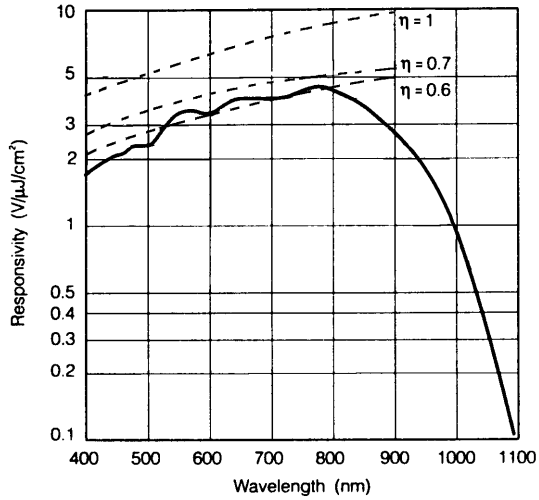
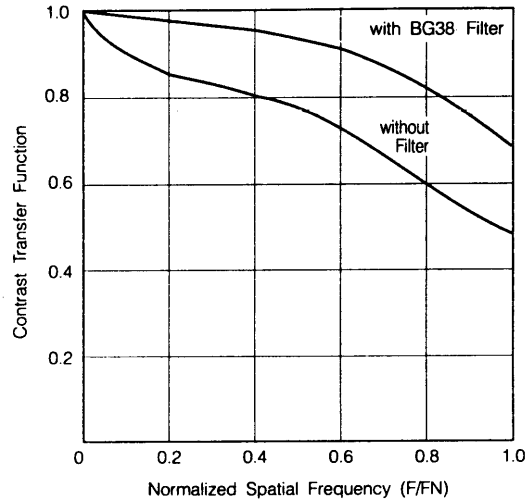


Figure 3. CTF Typical Curves (2854 K Source)



Electro-optical Performance Without Infrared Cut-off Filtering

The TH7841A special semiconductor process exploits the silicon's high near infrared sensitivity while maintaining good imaging performance in terms of response uniformity and resolution. Typical changes in performance with and without IR filtering are summarized below.

	With IR Cut-off Filter	No IR Cut-off Filter
Average Video Signal Due To a Given Scene Illumination	V_{OS}	V_{OS} x 4
PRNU (Single Defects Excluded)	±5%	±5%
CTF at Nyquist Frequency	70%	50%

Complementary Operating Modes

The TH7841A may be used in several configurations in regards to video output sampling and charge sensing reset.

1. Sampling options

Inhibition of internal sampling pulses allows two possibilities:

a. no sampling: video output delivered in unsampled form,

b. sampling by external clocks: external sampling pulses directly applied to Φ_{ECHA}, Φ_{ECHB} inputs.

If internal sampling clocks $S\Phi_{ECHA}$ and $S\Phi_{ECHB}$ are not used, it is recommended to unpower the corresponding clock drivers, as this will greatly reduce on-chip power consumption.

2. External reset position

The position and period of the charge reset clocks may be optimized by using external clocks on Φ_{RA} and Φ_{RB} inputs. This is especially interesting to optimize the video outputs for Correlated Double Sampling (in order to reduce noise and improve S/N Ratio).

Control signals to be applied in the different configurations are shown in Table 6.

Table 6. Selection of Operating Modes

Option	Implementation	Note
No Sampling	Φ_{ECHA} (3) and Φ_{ECHB} (25) Connected to VDD $S\Phi_{ECHA}$ (4) and $S\Phi_{ECHB}$ (24) Unconnected V_{INH} (16) Connected to V_{DD}	(1)
Sampling By External Clocks	Sampling Clocks Connected to Φ_{ECHA} - Φ_{ECHB} $S\Phi_{ECHA}$ and $S\Phi_{ECHB}$ Unconnected V_{INH} (16) Connected to V_{DD}	See Figure 4 for sampling clock timing (1)
Reset Control By External Clocks	Ext. Φ_{RA} on Φ_{RA} (5) Input Ext. Φ_{RB} on Φ_{RB} (21) Input	See Figure 4 for reset clock timing

Note: 1. Drain supply current I_{DD} decreases from 10 mA to 8 mA typically when internal sampling clock is disabled (V_{INH} = V_{DD} = 15V).

Table 7. External ΦRA, ΦRB, ΦECHA, ΦECHB Clocks Characteristics

Parameter	Symbol	Logic	Values			Unit
			Min	Typ	Max	
External Reset Clock Sampling Clock	Φ_{RA}, Φ_{RB}, Φ_{ECHA}, Φ_{ECHB}	High	12	13	14	V
		Low	0.0	0.4	0.6	V
Reset And Sampling Clock Capacitance	$C\Phi_{RA}$ $C\Phi_{RB}$ $C\Phi_{ECHA}$ $C\Phi_{ECHB}$			10	15	pF

Insertion of a serial resistor (typically 100Ω) at the driver output avoids spurious negative transients.

Figure 4. Timing Diagram — Clocks and Video Output Timing Diagram With and Without On-chip Sampling

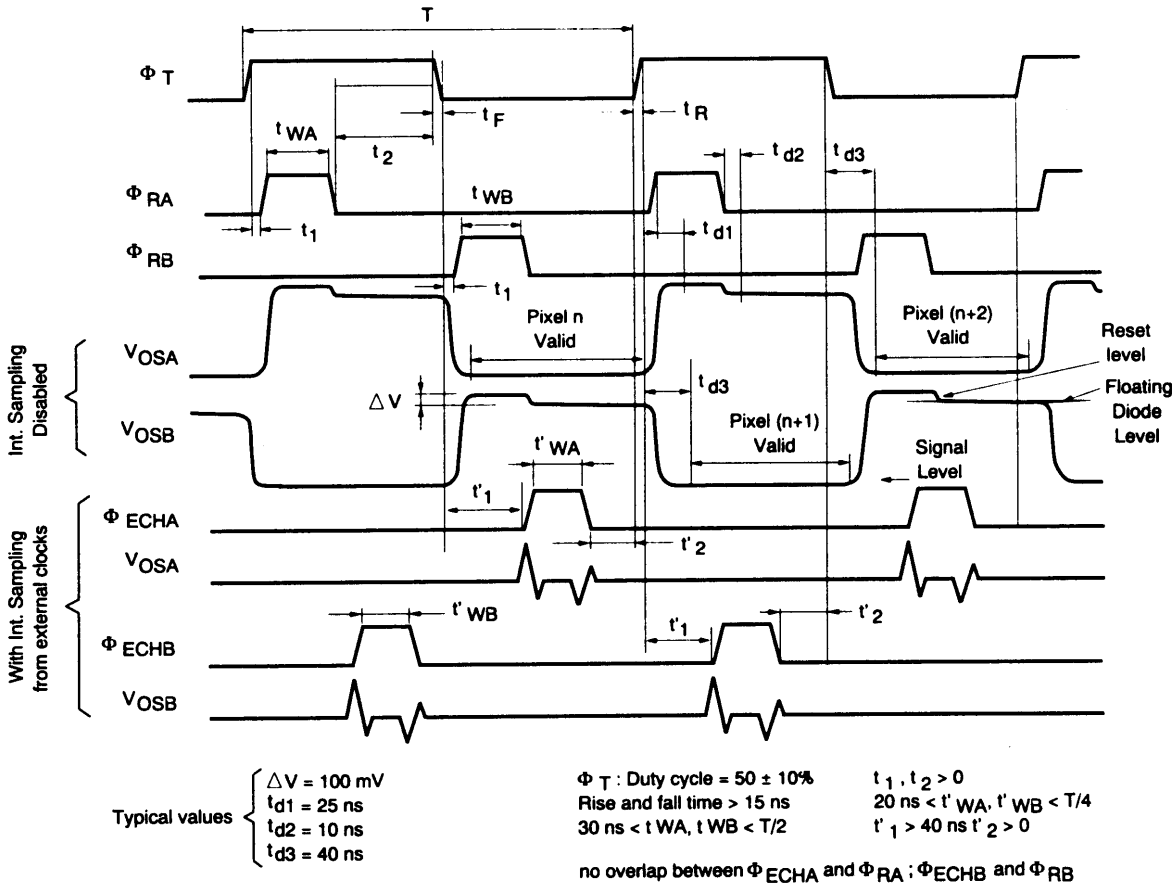


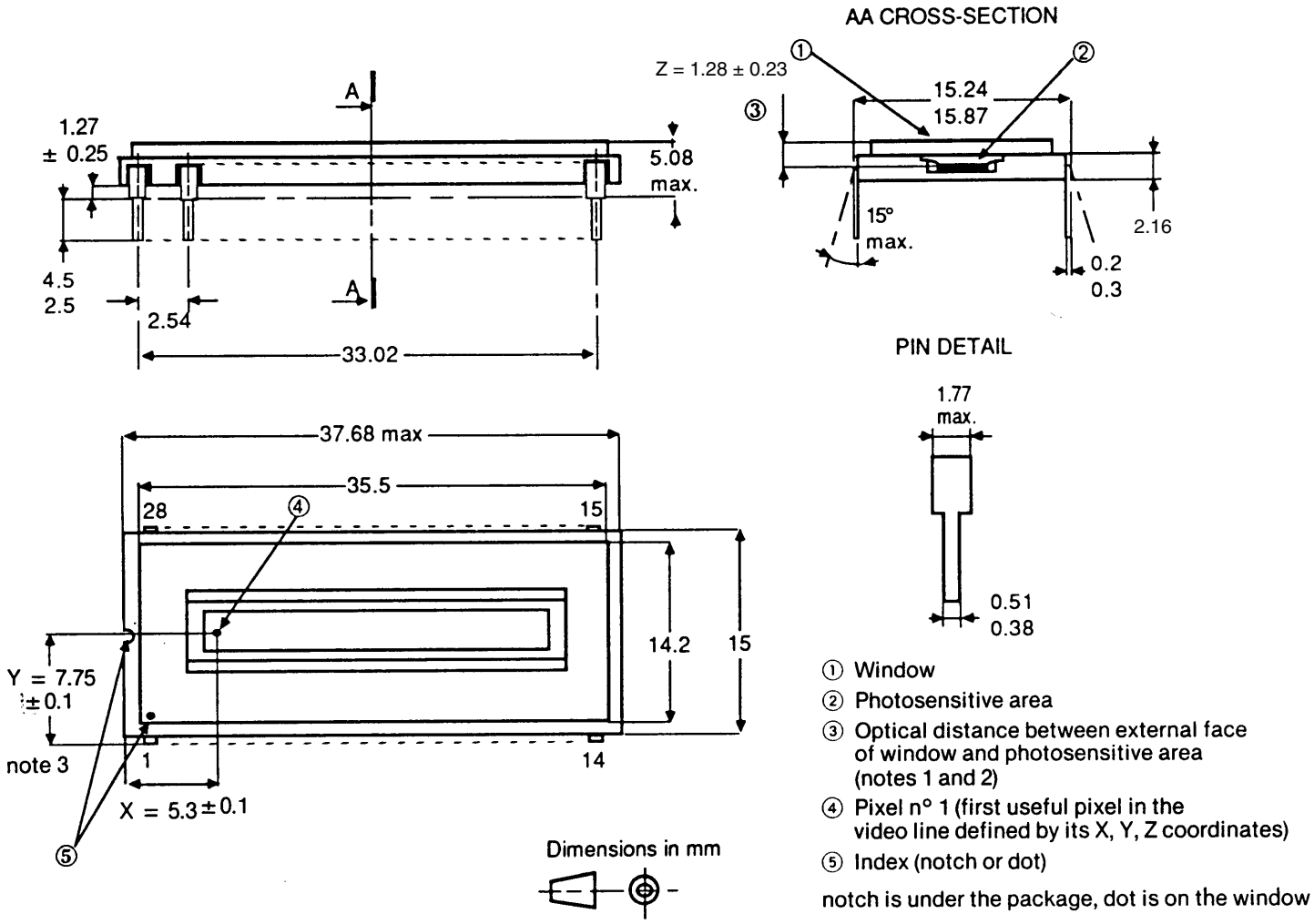
Table 8. Performance Improvement with External Φ_{RA}, Φ_{RB} Configuration[1][2]

Parameter	Symbol	Values (Typ)	Unit
Saturation Output Voltage	V_{SAT}	2.0	V
Responsivity	R	5.0	V/µJ/cm^2
Dynamic Range	DR	8,000	

Notes: 1. Electro-optical performances obtained with complementary modes are not guaranteed for standard products.
2. The Conversion factor is typically 1.8 µV/e-.

Packaging Information

TH 7841A with standard window.



Notes:
1. If an optical reference is needed, it is recommended to use the window face plane.
2. Variation of Z (azimuth) on the photosensitive area of a device is ≤ 0.1 mm
3. Variation of Y between the first and the last pixel of the linear area is ≤ ±130 µm.

Ordering Code

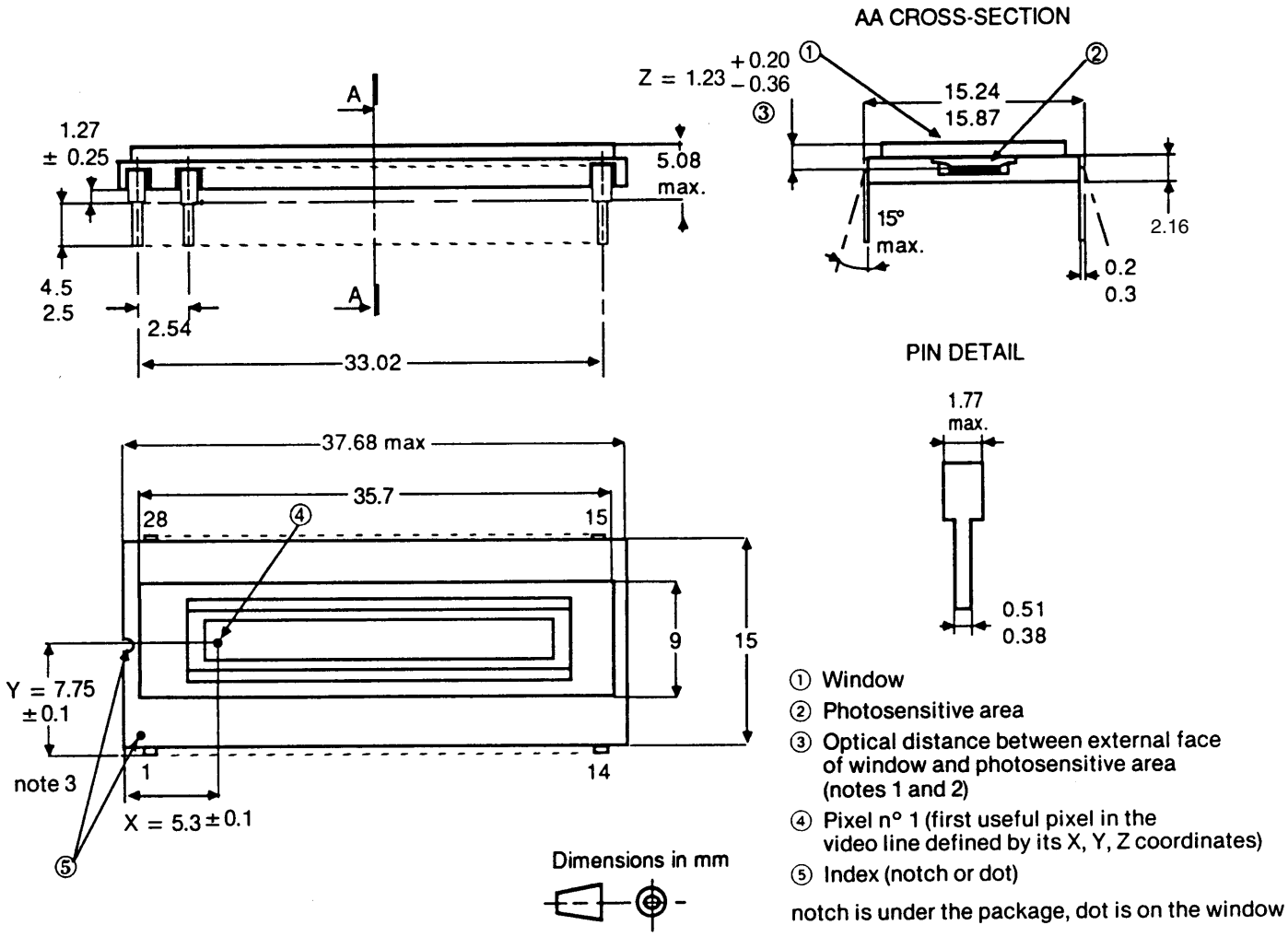
The ordering code is: TH7841 ACC

TH7841A With Antireflective Window

Improvements in the bandwidth 450-750 nm:

- 5% increase in responsivity (typical value: 3.0 V/µJ/cm^2).
- limitation of the parasitic reflections.

Package Drawing



Notes: 1. If an optical reference is needed, it is recommended to use the window face plane.
2. Variation of Z (azimuth) on the photosensitive area of a device is ≤ 0.1 mm
3. Variation of Y between the first and the last pixel of the linear area is ≤ ±130 µm.

Ordering Code

The ordering code is: TH7841 ACC-R

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